

Revision History

Revision 0.1 (Jul. 2010)

- First release.

512Mb (8M×4Bank×16) Double DATA RATE SDRAM

Features

- Internal Double-Data-Rate architecture with 2 accesses per clock cycle.
- 1.8V ±0.1V VDD/VDDQ
- 1.8V LV-COMS compatible I/O
- Burst Length (B/L) of 2, 4, 8, 16
- 3 Clock read latency (CL3)
- Bi-directional, intermittent data strobe (DQS)
- All inputs except data and DM are sampled at the positive edge of the system clock.
- Data Mask (DM) for write data
- Sequential & Interleaved Burst type available
- Auto Precharge option for each burst accesses
- DQS edge-aligned with data for Read cycles
- DQS center-aligned with data for Write cycles
- No DLL; CK to DQS is not synchronized
- Deep power down mode
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self-Refresh (TCSR) by built-in temperature sensor
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms

Description

The EM42BM1684LBB is a Double Data Rate Synchronous DRAM fabricated with ultra-high performance CMOS process containing 536,870,912 bits which organized as 8Meg words x 4 banks by 16 bits.

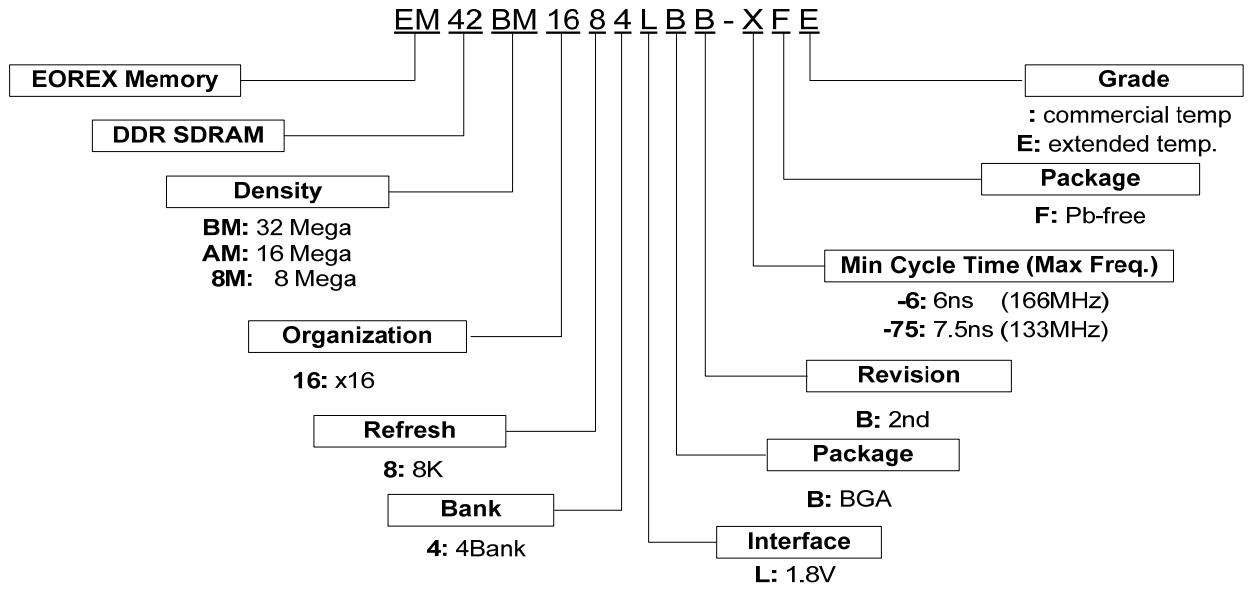
The 512Mb DDR SDRAM uses double data rate architecture to accomplish high-speed operation.

The data path internally prefetches multiple bits and It transfers the data for both rising and falling edges of the system clock. It means the doubled data bandwidth can be achieved at the I/O pins.

Available packages: FBGA-60B (10mmx8mm).

Ordering Information

Part No	Organization	Max. Freq	Package	Grade	Pb
EM42BM1684LBB-75F	32M X 16	133MHz/DDR266 @CL3	BGA-60B	Commercial.	Free
EM42BM1684LBB-6F	32M X 16	166MHz/DDR333 @CL3	BGA-60B	Commercial	Free
EM42BM1684LBB-75FE	32M X 16	133MHz/DDR266 @CL3	BGA-60B	Extend Temp.	Free
EM42BM1684LBB-6FE	32M X 16	166MHz/DDR333 @CL3	BGA-60B	Extend Temp.	Free



* EOREX reserves the right to change products or specification without notice.

Pin Assignment

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
VDDQ	DQ13	DQ14	B	DQ1	DQ2	VSSQ
VSSQ	DQ11	DQ12	C	DQ3	DQ4	VDDQ
VDDQ	DQ9	DQ10	D	DQ5	DQ6	VSSQ
VSSQ	UDQS	DQ8	E	DQ7	LDQS	VDDQ
VSS	UDM	NC	F	NC	LDM	VDD
CKE	CLK	/CLK	G	/WE	/CAS	/RAS
A9	A11	A12	H	/CS	BA0	BA1
A6	A7	A8	J	A10/AP	A0	A1
VSS	A4	A5	K	A2	A3	VDD

60ball FBGA / (10mm x 8mm)

Pin Description (Simplified)

Pin	Name	Function
G2,G3	CLK,/CLK	(System Clock) Clock input active on the Positive rising edge except for DQ and DM are active on both edge of the DQS. CLK and /CLK are differential clock inputs.
H8	/CS	(Chip Select) /CS enables the command decoder when "L" and disable the command decoder when "H". The new command are over-Looked when the command decoder is disabled but previous operation will still continue.
H1	CKE	(Clock Enable) Activates the CLK when "H" and deactivates when "L". When deactivate the clock, CKE low signifies the power down or self refresh mode.
K7,L8,L7,M8,M2, L3,L2,K3,K2,J3,K8, J2,H2	A0~12	(Address) Row address (A0 to A12) and Column address (CA0 to CA9) are multiplexed on the same pin. CA10 defines auto precharge at Column address.
J8,J7	BA0, BA1	(Bank Address) Selects which bank is to be active.
H7	/RAS	(Row Address Strobe) Latches Row Addresses on the positive rising edge of the CLK with /RAS "L". Enables row access & pre-charge.
G8	/CAS	(Column Address Strobe) Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
G7	/WE	(Write Enable) Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
E7,E3	LDQS, UDQS	(Data Input/Output) Data Inputs and Outputs are synchronized with both edge of DQS.
F7,F8	LDM,UDM	(Data Input/Output Mask) DM controls data inputs. LDM corresponds to the data on DQ0~DQ7.UDM corresponds to the data on DQ8~DQ15.
A8,B9,B7,C9 C7,D9,D7,E9 E1,D3,D1,C3 C1,B3,B1,A2	DQ0~15	(Data Input/Output) Data inputs and outputs are multiplexed on the same pin.
A7,F8,M7/ A3,F2,M3	V _{DD} /V _{SS}	(Power Supply/Ground) V _{DD} and V _{SS} are power supply pins for internal circuits.
A9,B1,C8,D2,E8 / A1,B8,C2,D8,E2,	V _{DDQ} /V _{SSQ}	(Power Supply/Ground) V _{DDQ} and V _{SSQ} are power supply pins for the output buffers.
F1,F9	NC/RFU	(No Connection/Reserved for Future Use) This pin is recommended to be left No Connection on the device.

Absolute Maximum Rating

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.5 ~ +2.7	V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.5 ~ +2.7	V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +70
		Extended	-25 ~ +85
T_{STG}	Storage Temperature Range	-55 ~ +125	°C
P_D	Power Dissipation	0.7	W
I_{OS}	Short Circuit Current	50	mA

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance ($V_{CC}=1.8V \pm 0.1V, f=1MHz, T_A=25^\circ C$)

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{CLK}	Clock Capacitance	1.5	-	3.0	pF
C_I	Input Capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML, DQMU	1.5	-	3.0	pF
C_O	Input/Output Capacitance	3.0	-	5.0	pF

Recommended DC Operating Conditions ($T_A=0^\circ C \sim 70^\circ C$)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.7	1.8	1.95	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	1.7	1.8	1.95	V
V_{IH}	Input Logic High Voltage	$0.7 * V_{DDQ}$	-	$V_{DDQ} + 0.3$	V
V_{IL}	Input Logic Low Voltage	-0.3	-	$0.3 * V_{DDQ}$	V

Note: * All voltages referred to V_{SS} .

Recommended DC Operating Conditions

($V_{DD}=1.8V\pm 0.1V$, $T_A=0^{\circ}C \sim 70^{\circ}C$)

Symbol	Parameter	Test Conditions	Max.		Units
			-6	-75	
I_{DD1}	Operating Current <i>(Note 1)</i>	$t_{CK}=t_{CK}(\text{min.})$, CKE & /CS are high $t_{RC}=t_{RC}(\text{min.})$, One bank active Input signals are switching; DQ stable	70	65	mA
I_{DD2P}	Precharge Standby Current (Power Down Mode)	CKE is low, $t_{CK}=t_{CK}(\text{min.})$, /CS is high Input signals are switching; DQ stable All banks idle	0.3	0.3	mA
I_{DD2N}	Precharge Standby Current (Non-power Down Mode)	CKE is high, $t_{CK}=t_{CK}(\text{min.})$, /CS is high Input signals are switching; DQ stable All banks idle	5	5	mA
I_{DD3P}	Active Standby Current (Power Down Mode)	CKE is low, $t_{CK}=t_{CK}(\text{min.})$, /CS is high Input signals are switching; DQ stable One bank active	0.5	0.5	mA
I_{DD3N}	Active Standby Current (Non-power Down Mode)	CKE is high, $t_{CK}=t_{CK}(\text{min.})$, /CS is high Input signals are switching; DQ stable One bank active	15	15	mA
I_{DD4}	Operating Current (Burst Mode) <i>(Note 2)</i>	$t_{CK}=t_{CK}(\text{min.})$, $I_{OL}=0\text{mA}$, BL=4, CL=3 Continuous read burst, input signals are switching, 50% data change per burst One bank active	110	100	mA
		$t_{CK}=t_{CK}(\text{min.})$, BL=4 Continuous write burst, input signals are switching, 50% data change per burst One bank active	100	90	
I_{DD5}	Refresh Current <i>(Note 3)</i>	$t_{RFC}=t_{RFC}(\text{min.})$, $t_{CK}=t_{CK}(\text{min.})$ CKE is high, burst refresh Input signals are switching; DQ stable	90	90	mA
I_{DD6}	Self Refresh Current	CKE ≤ 0.2 , Full Array, Internal TCSR = 85°C	3	3	mA
I_{DD8}	Deep Power Down Mode Current		10	10	μA

*All voltages referenced to V_{SS} .

Note 1: I_{DD1} depends on output loading and cycle rates.

Specified values are obtained with the output open.

Input signals are changed only one time during $t_{CK}(\text{min.})$

Note 2: I_{DD4} depends on output loading and cycle rates.

Specified values are obtained with the output open.

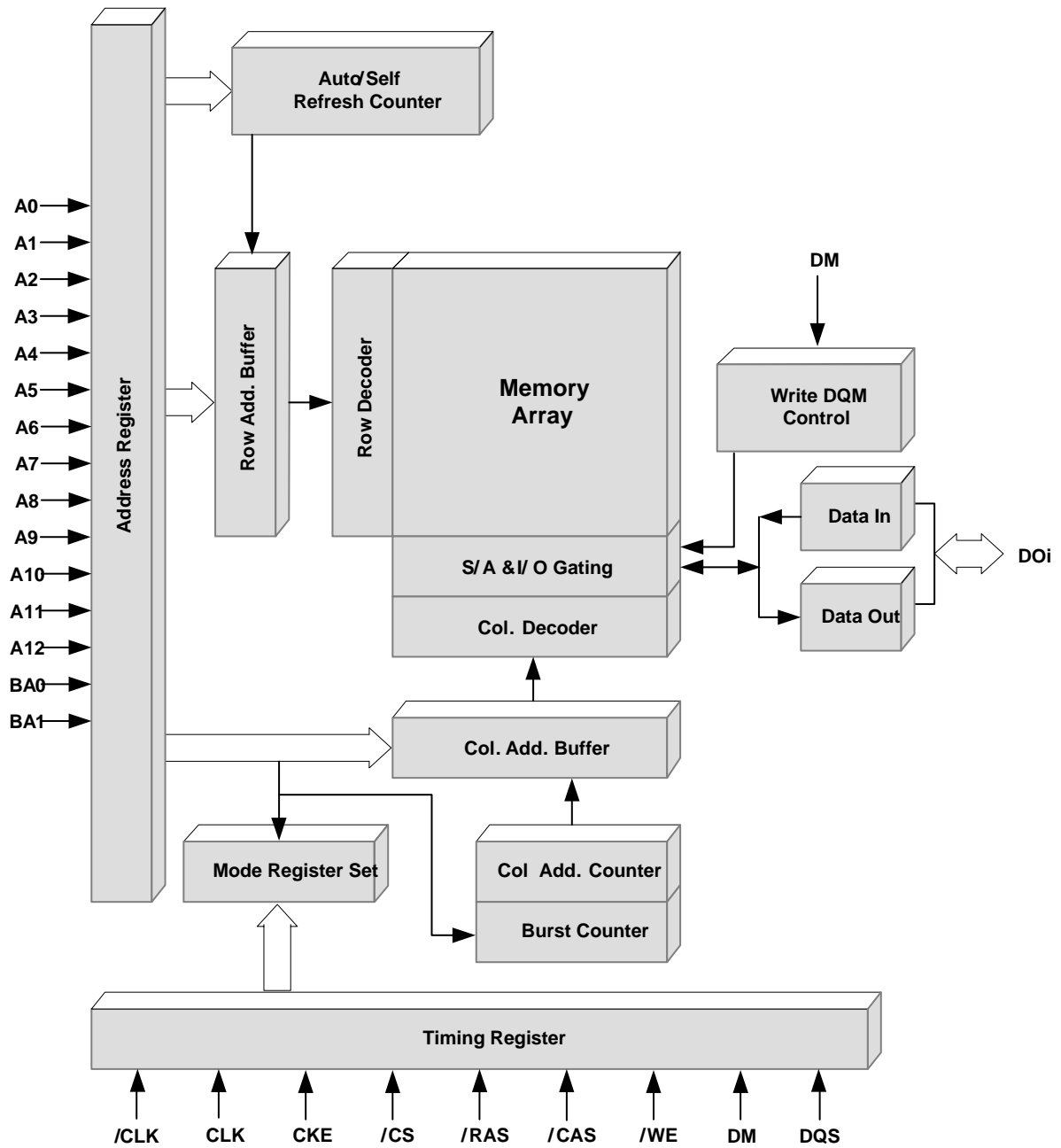
Input signals are changed only one time during $t_{CK}(\text{min.})$

Note 3: Min. of t_{RFC} (Auto refresh Row Cycle Times) is shown at AC Characteristics.

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{IL}	Input Leakage Current	$0 \leq V_I \leq V_{DDQ}$, $V_{DDQ} = V_{DD}$ All other pins not under test=0V	-2	-	+2	μA
I_{OL}	Output Leakage Current	$0 \leq V_O \leq V_{DDQ}$, D_{OUT} is disabled	-1.5	-	+1.5	μA
V_{OH}	High Level Output Voltage	$I_O = -0.1mA$	$0.9 * V_{DDQ}$	-	-	V
V_{OL}	Low Level Output Voltage	$I_O = +0.1mA$	-	-	$0.1 * V_{DDQ}$	V

Block Diagram



AC Operating Conditions

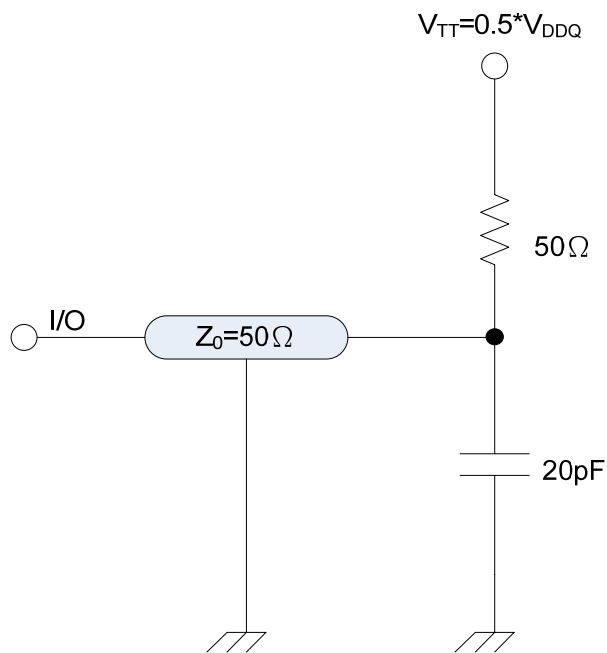
($V_{DD}=1.8V \pm 0.1V$, $T_A=0^{\circ}C \sim 70^{\circ}C$)

Symbol	Parameters	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH voltage: DQ	$0.8 \cdot V_{DDQ}$	-	$V_{DDQ} + 0.3$	V
V_{IL}	Input LOW voltage: DQ	-0.3	-	$0.2 \cdot V_{DDQ}$	V
V_{IX}	Clock input crossing point voltage: CLK & /CLK	$0.4 \cdot V_{DDQ}$	-	$0.6 \cdot V_{DDQ}$	V

Test Conditions

($V_{DD}=1.8V \pm 0.1V$, $T_A=0^{\circ}C \sim 70^{\circ}C$)

Item	Conditions
Output Reference Level	$0.5 \cdot V_{DDQ}$ (V)
Output Load	See diagram as below
Input Signal Level	$0.8 \cdot V_{DDQ} / 0.2 \cdot V_{DDQ}$ (V)
Transition Time of Input Signals	1/1 (ns)
Input Reference Level	$0.5 \cdot V_{DDQ}$ (V)



AC Operating Test Characteristics(V_{DD}=1.8V±0.1V, T_A=0°C ~70°C)

Symbol	Parameter	-6		-7.5		Units
		Min.	Max.	Min.	Max.	
t _{DQCK}	DQ output access from CLK,/CLK	2	5.5	2	6	ns
t _{DQSCK}	DQS output access from CLK,/CLK	2	5.5	2	6	ns
t _{CL} ,t _{CH}	CL low/high level width	0.45	0.55	0.45	0.55	t _{CK}
t _{CK}	Clock Cycle Time (CL3)	6	100	7.5	100	ns
t _{DH} ,t _{DS}	DQ and DM hold/setup time	0.6		0.8		ns
t _{DIPW}	DQ and DM input pulse width for each input	1.2		1.75		ns
t _{HZ} ,t _{LZ}	Data out high/low impedance time from CLK, /CLK	1	5.5	1	6	ns
t _{DQSQ}	DQS-DQ skew for associated DQ signal	-	0.5	-	0.6	ns
t _{DQSS}	Write command to first latching DQS transition	0.75	1.25	0.75	1.25	t _{CK}
t _{DQSL} , t _{DQSH}	DQS input valid window	0.4	0.6	0.4	0.6	t _{CK}
t _{MRD}	Mode Register Set command cycle time	2	-	2	-	t _{CK}
t _{WPRES}	Write Preamble setup time	0	-	0	-	ns
t _{WPRESH}	Write Preamble hold time	0.25	-	0.25	-	t _{CK}
t _{WPST}	Write Preamble	0.4	0.6	0.4	0.6	t _{CK}
t _{IH} ,t _{IS}	Address/control input hold/setup time	1.1	-	1.3	-	ns
t _{RPRE}	Read Preamble	0.9	1.1	0.9	1.1	t _{CK}

AC Operating Test Characteristics (Continued)

($V_{DD}=1.8V\pm 0.1V$, $T_A=0^{\circ}C \sim 70^{\circ}C$)

Symbol	Parameter	-6		-75		Units
		Min.	Max.	Min.	Max.	
t_{RPST}	Read Postamble	0.4	0.6	0.4	0.6	t_{CK}
t_{RAS}	Active to Precharge command period	42	100k	45	100k	ns
t_{RC}	Active to Active command period	60	-	67.5	-	ns
t_{RFC}	Auto Refresh Row Cycle Time	110	-	110	-	ns
t_{RCD}	Active to Read or Write delay	18	-	22.5	-	ns
t_{RP}	Precharge command period	18	-	22.5	-	ns
t_{RRD}	Active bank A to B command period	12	-	15	-	ns
t_{CCD}	Column address to column address delay	1	-	1	-	t_{CK}
t_{HP}	Clock Half Period	t_{CL} (min) or t_{CH} (min)	-	t_{CL} (min) or t_{CH} (min)	-	t_{CK}
t_{QH}	Data hold time from DQS to earliest DQ edge	$t_{HP} - 0.6$		$t_{HP} - 0.75$		t_{CK}
T_{WR}	Write Recovery time	12	-	15	-	ns
t_{DAL}	Last Data input to active delay	Note 1				t_{CK}
t_{WTR}	Internal Write to Read command delay	2		1		t_{CK}
t_{XSR}	Exit Self Refresh to next valid command	200	-	200	-	ns
t_{XP}	Exit Power Down mode to first valid command	25	-	25	-	ns
t_{REF}	Refresh interval time	64	-	64	-	ms

Note 1: $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$, if the ratio is not an integer, take the next integer instead.

1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A12~A0
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	X	L	H	L	L	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	MRS	H	X	L	L	L	L	OP-Code		
Extended Mode Register Set	EMRS	H	X	L	L	L	L	OP-Code		

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. CKE Truth Table

Item	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Refresh	CBR Refresh	REF	H	H	L	L	L	H	X
	Self Refresh Entry	SELF	H	L	L	L	L	H	X
	Self Refresh Exit	-	L	H	L	H	H	H	X
Deep Power Down	Deep Power Down Entry	-	H	L	L	H	H	L	X
	Power Down Exit	-	L	H	H	X	X	X	X
Active PD	Entry	-	H	L	H	X	X	X	X
	Exit	-	L	H	X	X	X	X	X
Precharge PD	Entry	-	H	L	H	X	X	X	X
		-	H	L	L	H	H	H	X
	Exit	-	L	H	H	X	X	X	X
		-	L	H	L	H	H	H	X

H = High level, L = Low level, X = High or Low level (Don't care)

3. Operative Command Table

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT/BW	ILLEGAL (Note 1)
	L	L	H	H	BA/RA	ACT	Bank active, Latch RA
	L	L	H	L	BA, A10	PRE/PREA	NOP (Note 3)
	L	L	L	H	X	REFA	Auto refresh (Note 4)
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode register
Row Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA/CA/A10	READ/READA	Begin read, Latch CA, Determine auto-precharge
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write, Latch CA, Determine auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 1)
	L	L	H	L	BA/A10	PRE/PREA	Precharge/Precharge all
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	Terminal burst
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, Latch CA, Begin new read, Determine Auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 1)
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst, PrecharE
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst with DM="H", Latch CA, Begin read, Determine auto-precharge (Note 2)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, Latch CA, Begin new write, Determine auto-precharge (Note 2)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 1)
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst with DM="H", Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code,	MRS	ILLEGAL

3. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	BA/CA/A10	TERM	ILLEGAL
	L	H	L	X	BA/RA	READ/WRITE	ILLEGAL (Note 1)
	L	L	H	H	BA/A10	ACT	ILLEGAL (Note 1)
	L	L	H	L	X	PRE/PREA	ILLEGAL (Note 1)
	L	L	L	H	X	REFA	ILLEGAL
Write with AP	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL (Note 1)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 1)
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL (Note 1)
Pre-charging	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL (Note 1)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 1)
Row Activating	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP}) (Note 3)
	L	L	L	H	X	REFA	ILLEGAL
	H	X	X	X	X	DESL	NOP(Row active after t_{RCD})
	L	H	H	H	X	NOP	NOP(Row active after t_{RCD})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL (Note 1)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 1)
Row Activating	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL (Note 1)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

3. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA/CA/A10	READ	ILLEGAL (Note 1)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 1)
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL (Note 1)
	L	L	L	H	X	REFA	ILLEGAL
Refreshing	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT	ILLEGAL
	L	L	H	H	BA/RA	ACT	ILLEGAL
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP})
	L	L	L	H	X	REFA	ILLEGAL
L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 1: ILLEGAL to bank in specified states;

Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 2: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 3: NOP to bank precharging or in idle state. May precharge bank indicated by BA.

Note 4: ILLEGAL of any bank is not idle.

4. Command Truth Table for CKE

Current State	CKE		/CS	/R	/C	/W	Addr.	Action
	n-1	n						
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Self-Refresh
	L	H	L	H	H	H	X	Exist Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain self refresh)
Both bank precharge power down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Power down
	L	H	L	H	H	H	X	Exist Power down
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Power down)
All Banks Idle	H	H	X	X	X	X	X	Refer to function true table
	H	L	H	X	X	X	X	Enter power down mode ^(Note 3)
	H	L	L	H	H	H	X	Enter power down mode ^(Note 3)
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	RA	Row active/Bank active
	H	L	L	L	L	H	X	Enter self-refresh ^(Note 3)
	H	L	L	L	L	L	Op-Code	Mode register access
	H	L	L	L	L	L	Op-Code	Special mode register access
L	X	X	X	X	X	X	Refer to current state	
Any State Other than Listed above	H	H	X	X	X	X	X	Refer to command truth table

H = High level, L = Low level, X = High or Low level (Don't care)

Notes 1: After CKE's low to high transition to exist self refresh mode. And a time of $t_{rc}(\text{min})$ has to be Elapse after CKE's low to high transition to issue a new command.

Notes 2: CKE low to high transition is asynchronous as if restarts internal clock.

Notes 3: Power down and self refresh can be entered only from the idle state of all banks.

Recommended Power On and Initialization

The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs.

Provide power, the device core power (V_{DD}) and the device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that V_{DD} and V_{DDQ} are from the same power source. Also assert and hold Clock Enable (CKE) to a logic high level. Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.

After power on, an initial pause of 200 μ s is required followed by a precharge of all banks using the precharge command.

Provide NOPs or DESL commands for at least t_{RP} time.

Issue an auto-refresh command followed by NOPs or DESL command for at least t_{RFC} time. Issue the second auto-refresh command followed by NOPs or DESL command for at least t_{RFC} time.

Note as part of the initialization sequence there must be two auto-refresh commands issued.

Using the MRS command, load the base mode register. Set the desired operating modes.

Provide NOPs or DESL commands for at least t_{MRD} time.

Using the MRS command, program the extended mode register for the desired operating modes.

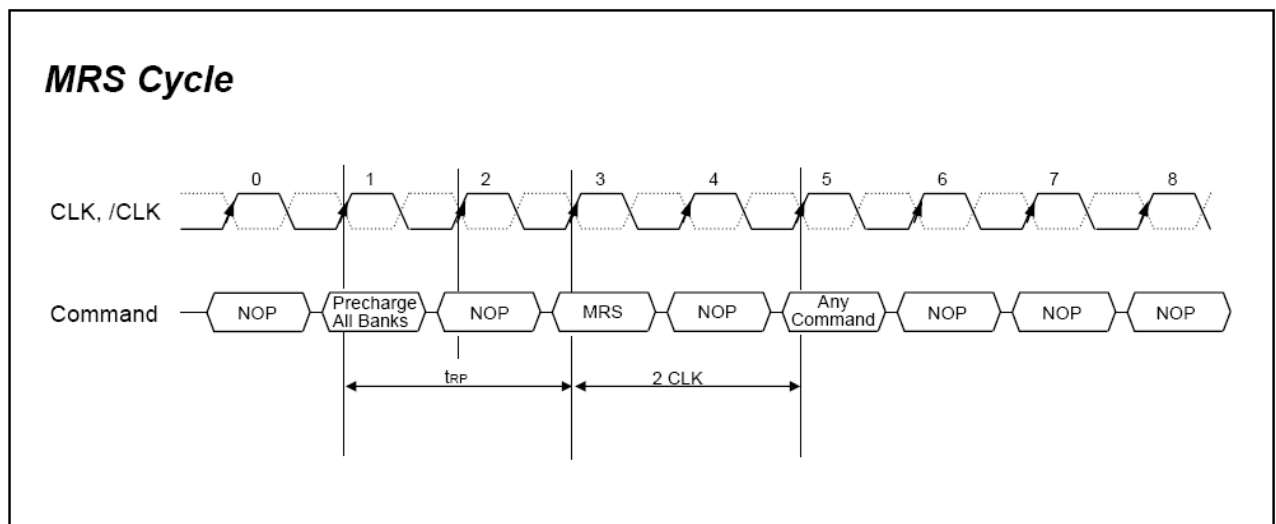
Provide NOP or DESL commands for at least t_{MRD} time.

Now it is ready for any valid command.

Mode Register Definition

Mode Register Set

The Mode Register stores the data for controlling various operating modes of a Mobile DDR SDRAM. It program include /CAS Latency, Burst Type, and Burst Length to make the Mobile DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed, the device enters Deep Power Down mode, or power is removed from the device. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0, BA1. (The device should have all banks idle with no burst in progress prior to writing into the mode register, CKE should be high) The state of the address pins A0-A12 in the same cycle in which /CS, /RAS, /CAS, /WE and BA0 are asserted low is written into the mode register. Two clock cycles are required to complete the write operation in the mode register. The mode register is divided into various fields depending on functionality. The burst length uses A0-A2, addressing mode uses A3, /CAS latency (read latency from column address) uses A4-A6.



Address input for Mode Register Set

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	CAS Latency			BT	Burst Latency		

Burst Type	A3
Sequential	0
Interleave	1

CAS Latency	A6	A5	A4
Reserve	0	0	0
Reserve	0	0	1
Reserve	0	1	0
3	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0
Reserve	1	1	1

Burst Latency	A2	A1	A0
Reserve	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0
Reserve	1	1	1

Burst Type (A3)

Burst Length	A3	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	X	0	0 1	0 1
	X	X	X	1	1 0	1 0
4	X	X	0	0	0 1 2 3	0 1 2 3
	X	X	0	1	1 2 3 0	1 0 3 2
	X	X	1	0	2 3 0 1	2 3 0 1
	X	X	1	1	3 0 1 2	3 2 1 0
8	X	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	X	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	X	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	X	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	X	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	X	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	X	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	X	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
16	0	0	0	0	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
	0	0	0	1	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0	1 0 3 2 5 4 7 6 9 8 11 10 13 12 15 14
	0	0	1	0	2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1	2 3 0 1 6 7 4 5 10 11 8 9 14 15 12 13
	0	0	1	1	3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2	3 2 1 0 7 6 5 4 11 10 9 8 15 14 13 12
	0	1	0	0	4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3	4 5 6 7 0 1 2 3 12 13 14 15 8 9 10 11
	0	1	0	1	5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4	5 4 7 6 1 0 3 2 13 12 15 14 9 8 11 10
	0	1	1	0	6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5	6 7 4 5 2 3 0 1 14 15 12 13 10 11 8 9
	0	1	1	1	7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8
	1	0	0	0	8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7
	1	0	0	1	9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8	9 8 11 10 13 12 15 14 1 0 3 2 5 4 7 6
	1	0	1	0	10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9	10 11 8 9 14 15 12 13 2 3 0 1 6 7 4 5
	1	0	1	1	11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10	11 10 9 8 15 14 13 12 3 2 1 0 7 6 5 4
	1	1	0	0	12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11	12 13 14 15 8 9 10 11 4 5 6 7 0 1 2 3
	1	1	0	1	13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12	13 12 15 14 9 8 11 10 5 4 7 6 1 0 3 2
	1	1	1	0	14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13	14 15 12 13 10 11 8 9 6 7 4 5 2 3 0 1
	1	1	1	1	15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

* Page length is a function of I/O organization and column addressing

Extended Mode Register Set (EMRS)

The Extended Mode Register is about to support Partial Array Self Refresh and Driver Strength. The Extended Mode Register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0, high on BA1. (The device should have all banks idle with no bursts in progress prior to writing into the Extended Mode Register, and CKE should be high) Values stored in the register will be retained until the register is reprogrammed, the device enters Deep Power Down mode, or power is removed from the device. The state of address pins A0-A12 and BA0, BA1 in the same cycle in which /CS, /RAS, /CAS and /WE are asserted low is written into the Extended Mode Register. Two clock cycles, t_{MRD} , are required to complete the write operation in the Extended Mode Register. All the other address pins, A3, A4, and A7 ~ A12 and BA0 must be set to low for proper EMRS operation. If the Extended Mode Register is not used in application, Driver Strength defaults to Full Strength; and PASR defaults to the Full Array.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	DS		0	0	PASR[2-0]		

Driver Strength	A6	A5
Full Strength	0	0
1/2 Strength	0	1
1/4 Strength	1	0
1/8 Strength	1	1

Active Section	A2	A1	A0
Full array	0	0	0
1/2 array (BA1= 0)	0	0	1
1/4 array (BA1=BA0=0)	0	1	0
Reserved	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

Output Drive Strength

The normal drive strength for all outputs is specified to be LV-CMOS. By setting EMRS specific parameter on A6 and A5, driving capability of data output drivers is selected.

Partial Array Self Refresh

For further power savings during Self Refresh, the PASR feature allows the controller to select the amount of memory that will be refreshed during Self Refresh. The refresh options are all banks (banks 0, 1, 2 and 3); two banks (bank 0 and 1); and one bank (bank 0). Write and Read commands can still affect any bank during standard operations, but only the selected banks will be refreshed during Self Refresh. Data in unselected banks will be lost.

Deep Power Down

Deep Power Down achieves maximum power reduction by eliminating the power of the whole memory array and surrounding circuitry. Data will not be retained in the memory storage array, the Mode Register, or the Extended Mode Register once the device enters Deep Power Down mode. This mode is entered by having all banks idle then /CS and /WE held Low with /RAS and /CAS held High at the rising edge of the clock, while CKE is Low. This mode is exited by asserting CKE High, applying only NOP commands for 200 microseconds, and then continuing with steps 4 through 11 of the Power Up and Initialization sequence.

Temperature Compensated Self Refresh

In order to reduce power consumption, a Mobile DDR SDRAM includes the internal temperature sensor and other circuitry to control Self Refresh operation automatically according to two temperature ranges: 40°C (max.) and 85°C (max.).

Temperature Range	Self Refresh Current (I_{CC6})			
	-E			Unit
	Full Array	1/2 Full Array	1/4 Full Array	
Max. 85°C	700	460	340	μA
Max. 40°C	490	350	280	μA

Package Description

60-Ball FBGA Package

