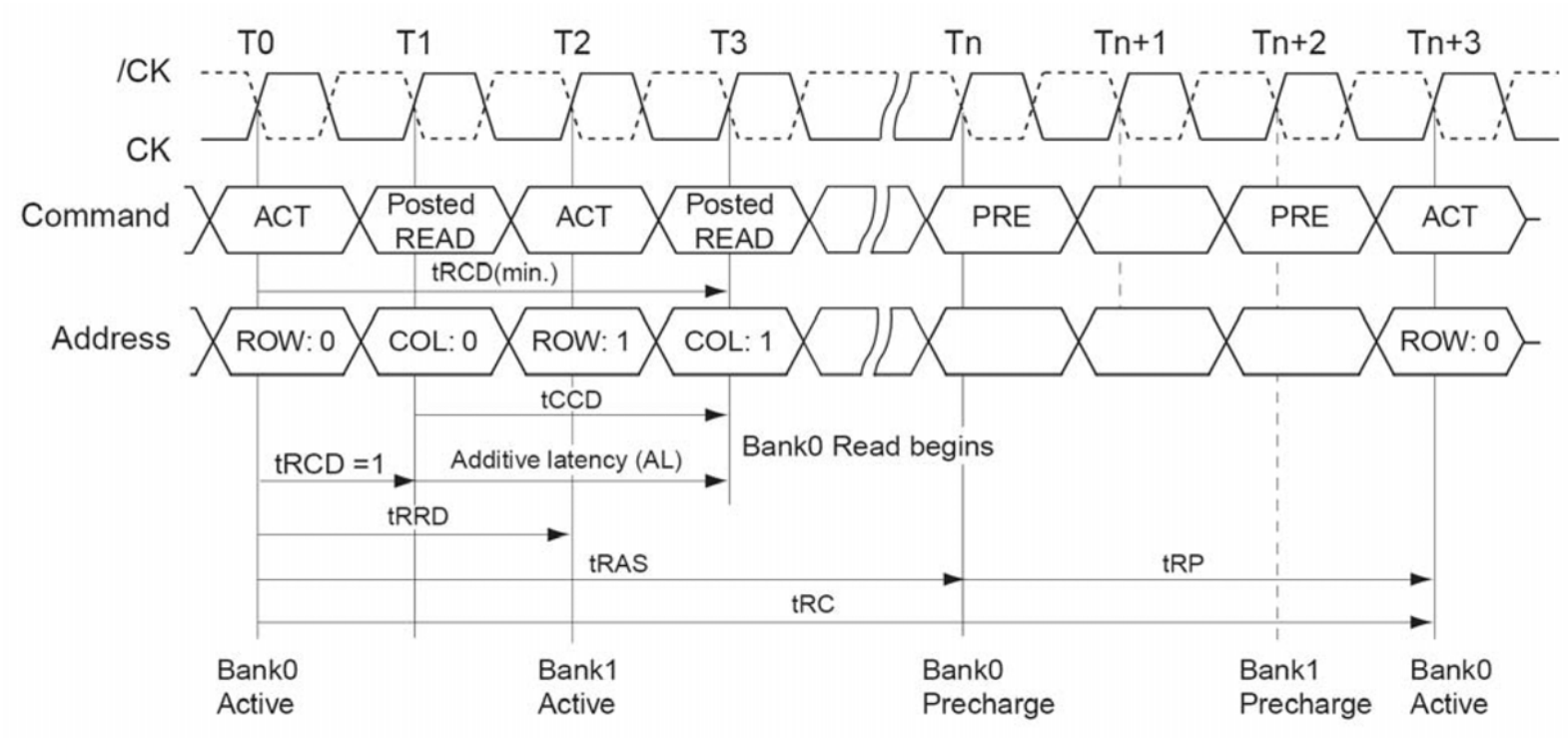
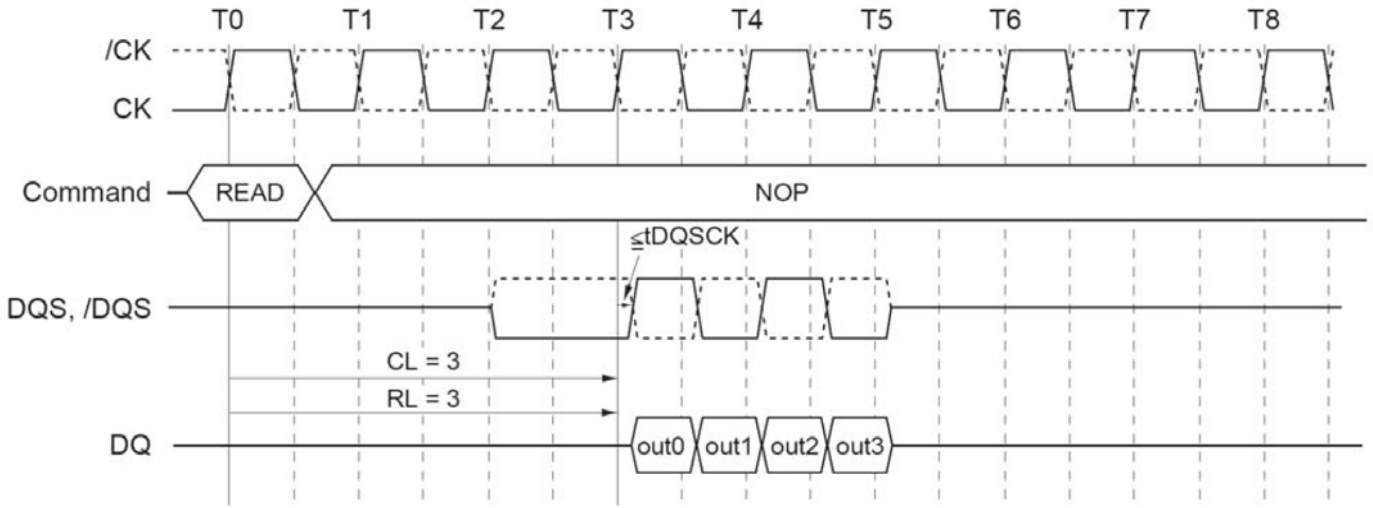
Contents

1. Bank Activate Command: tRCD=3, AL=2, tRP=3, tRRD=2

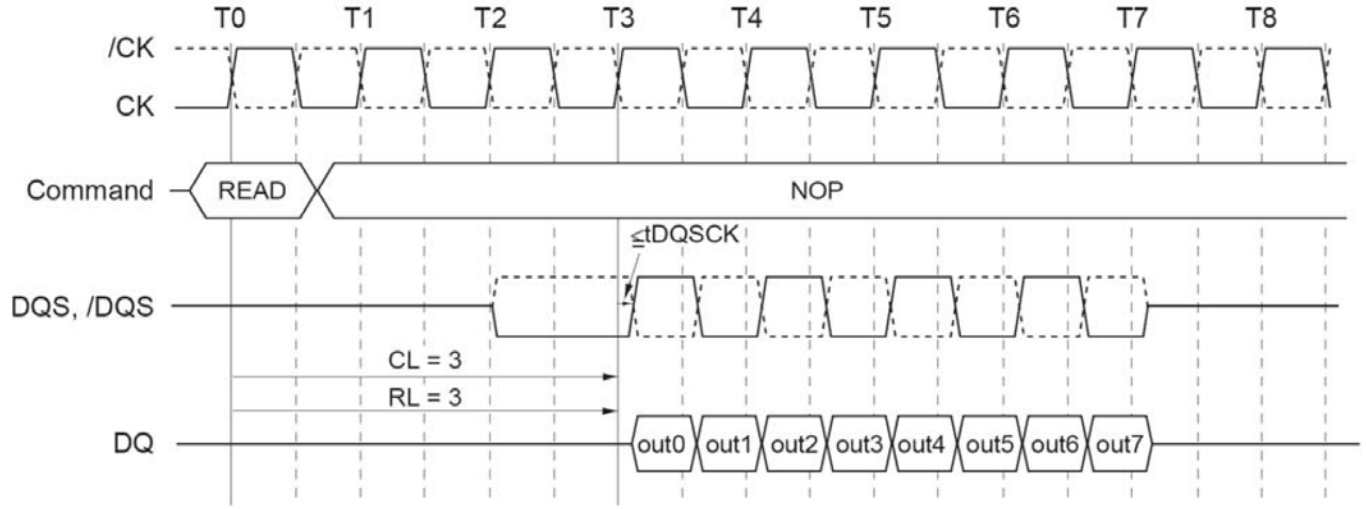


2. Burst Read Command:

CL=3, AL=0, RL=3, BL=4

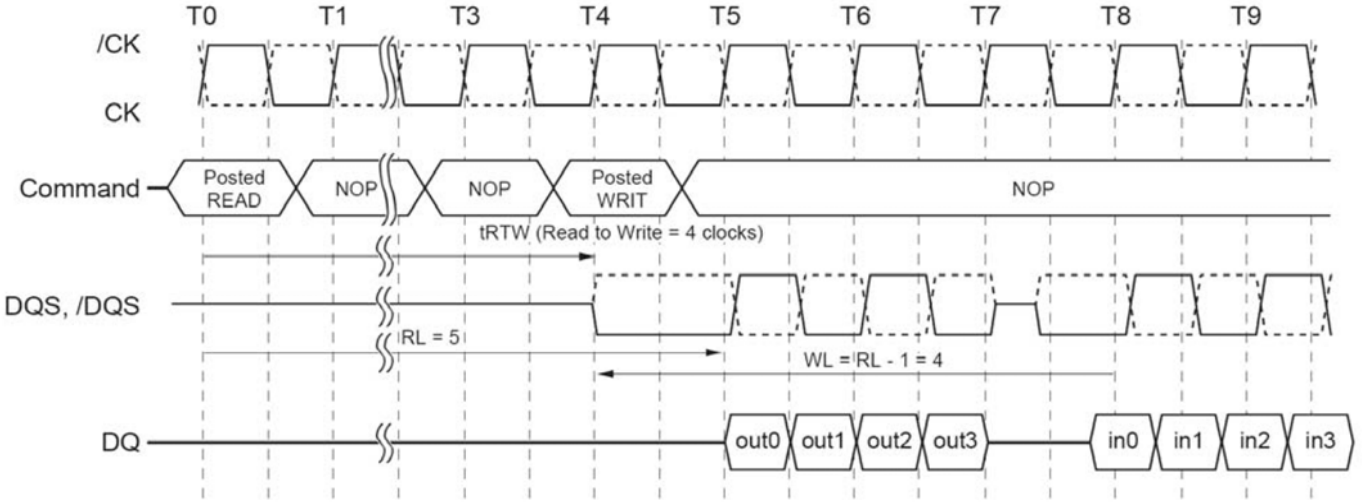


CL=3, AL=0, RL=3, BL=8



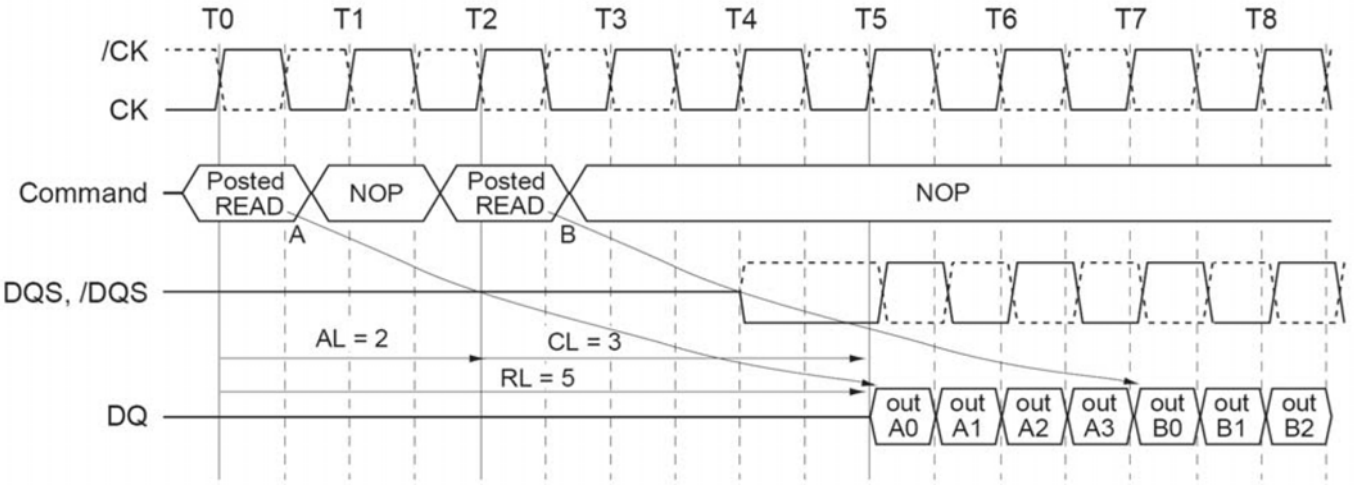
Burst Read Followed by Burst Write:

CL=3, RL=5, BL=4



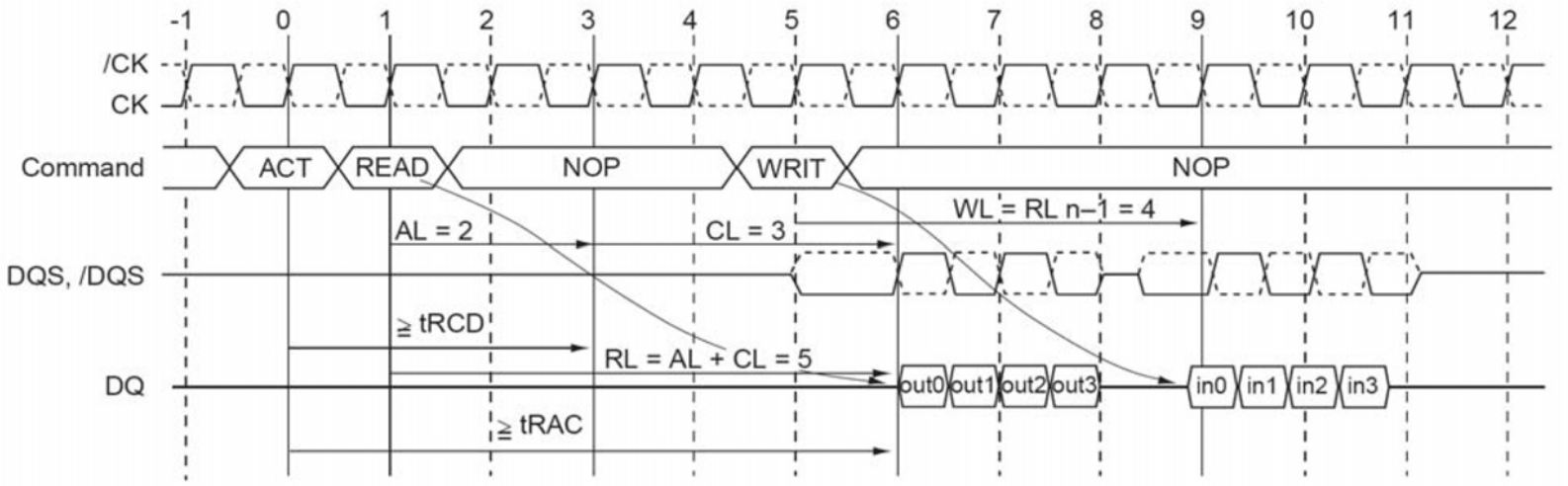
Seamless Burst Read:

CL=3, AL=2, RL=5, BL=4



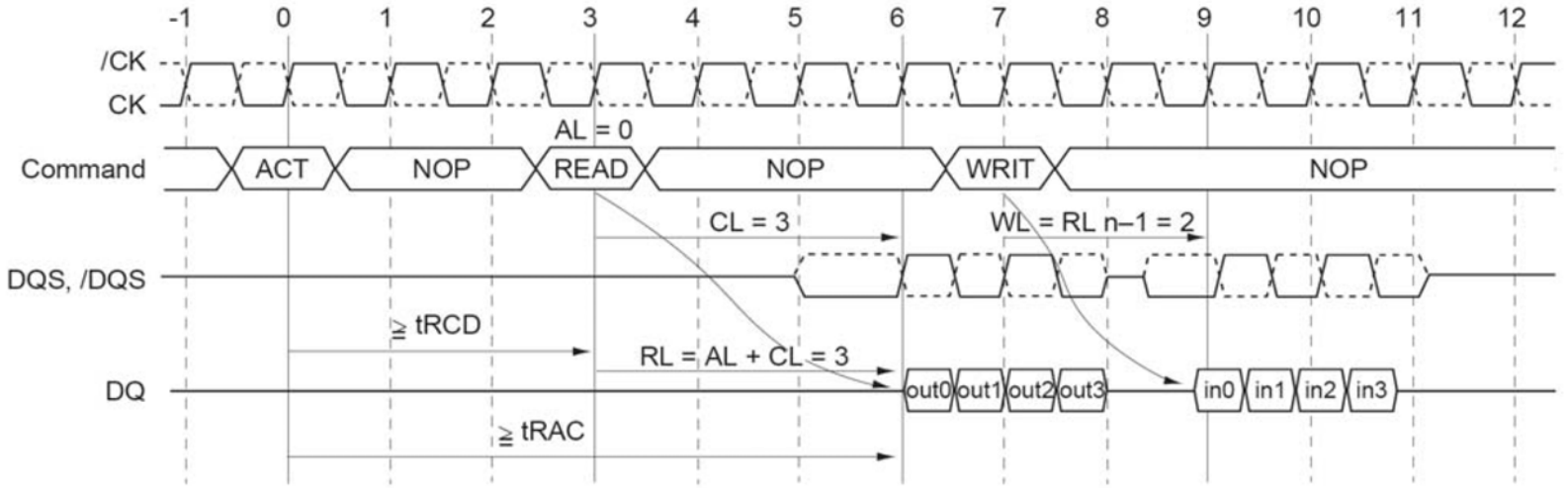
3. Read followed by a write to the same bank I: Activate to Read delay < tRCDmin

AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4



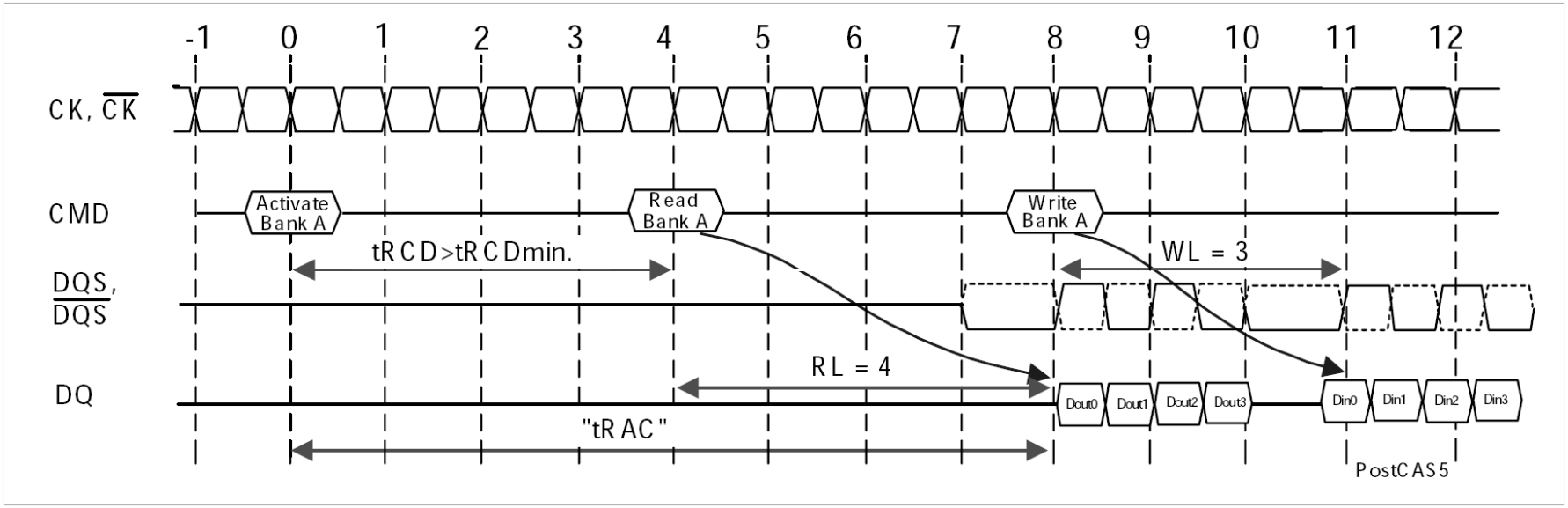
4. Read followed by a write to the same bank II: Activate to Read delay < tRCDmin

AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL -1) = 2, BL = 4

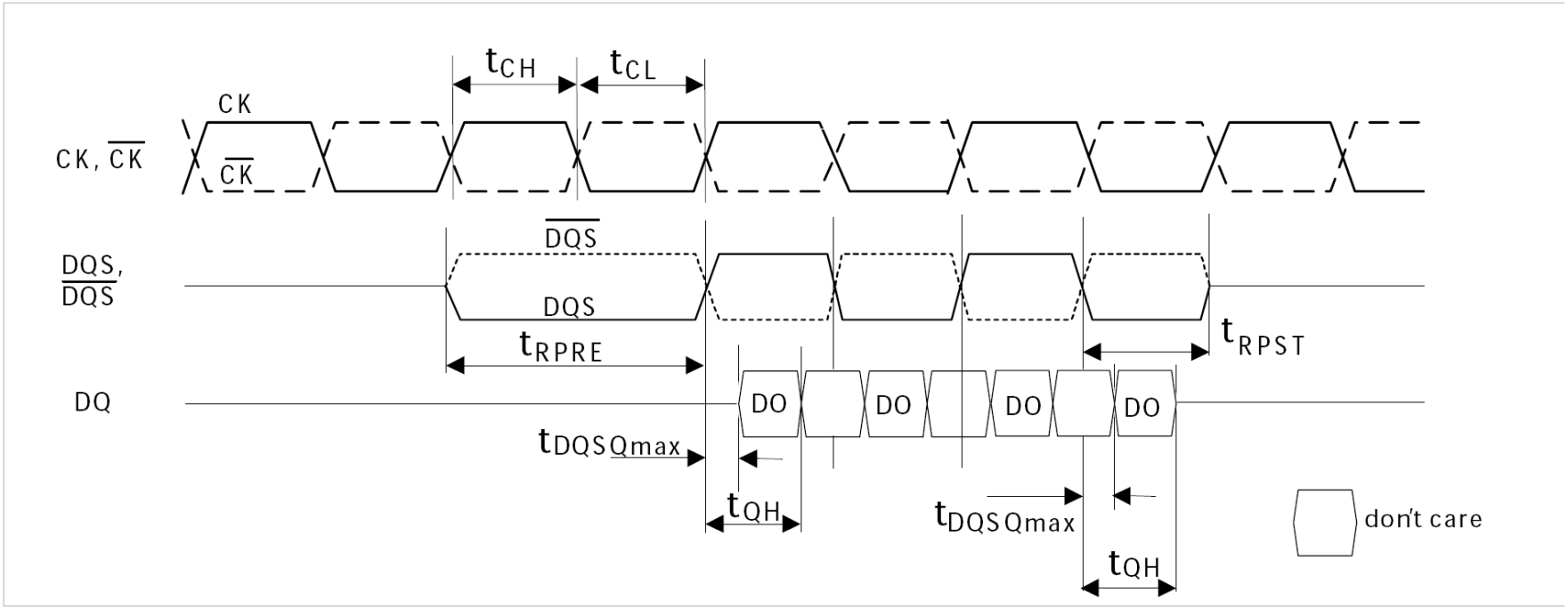


5. Read: Activate to Read delay < tRCDmin

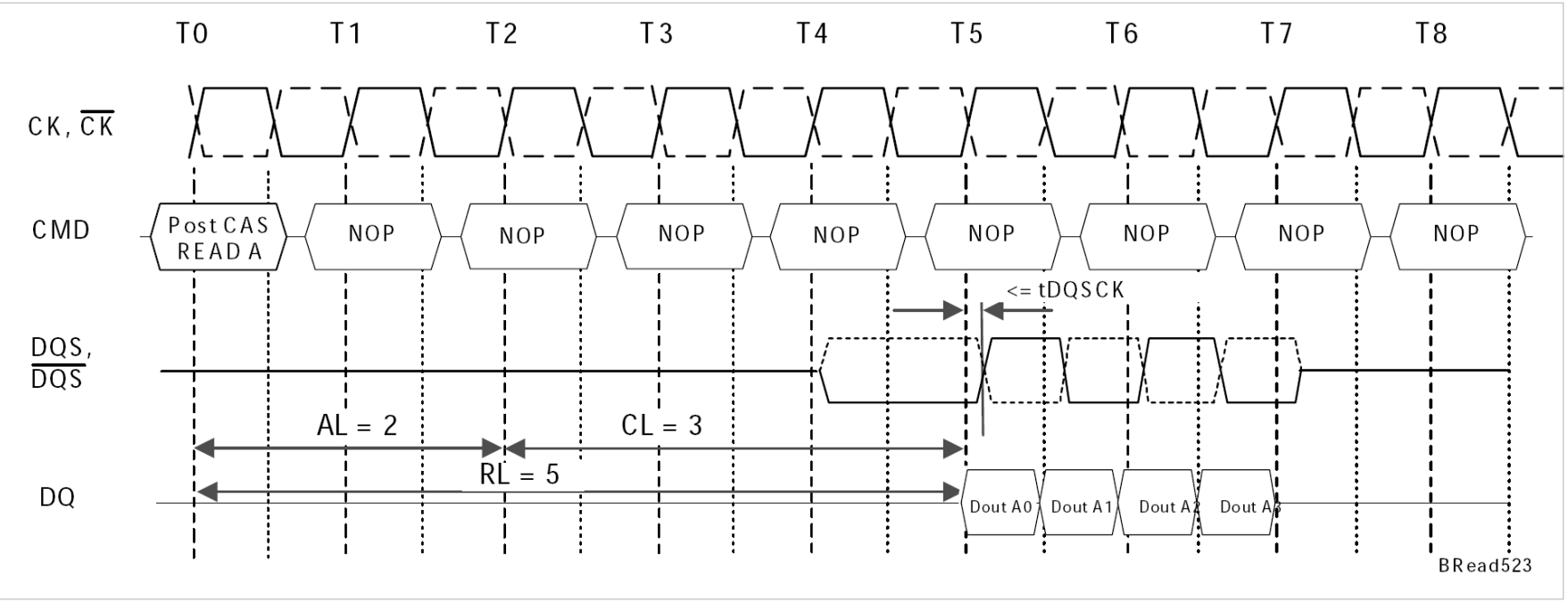
AL = 1, CL = 3, RL = 4, WL = 3, BL = 4



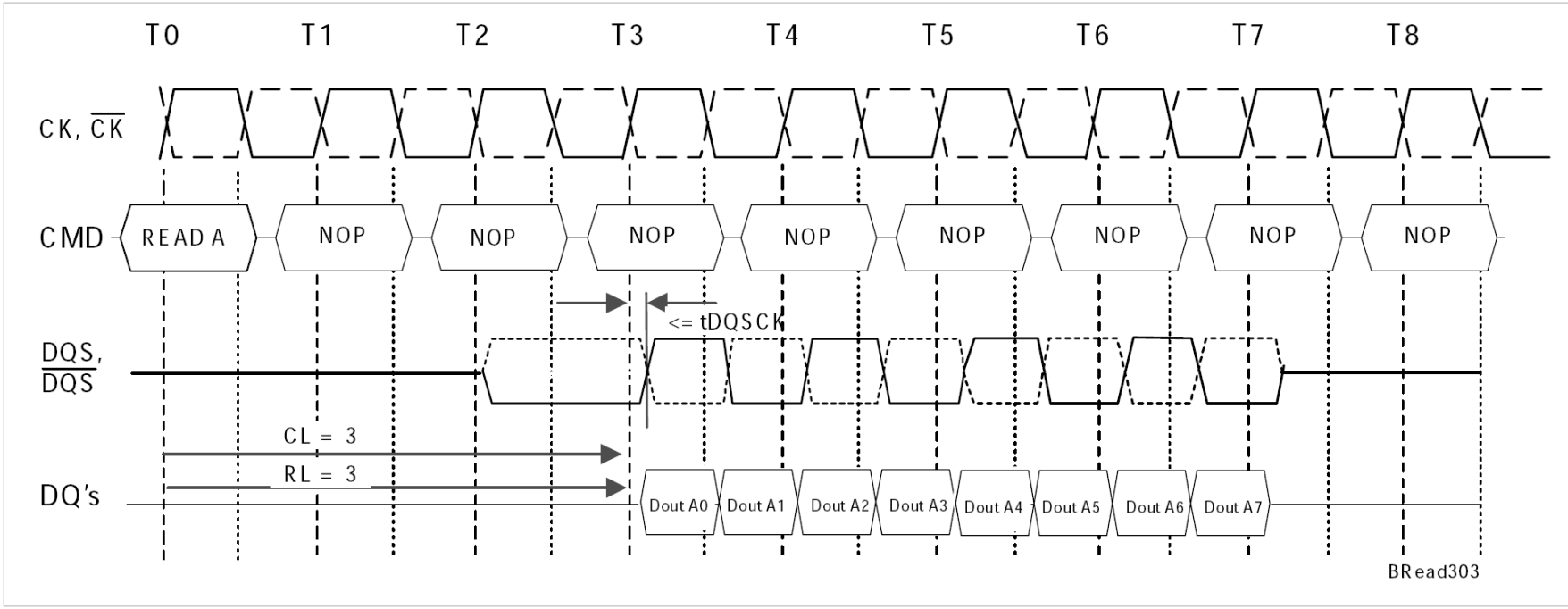
6. Basic Burst Read Timing



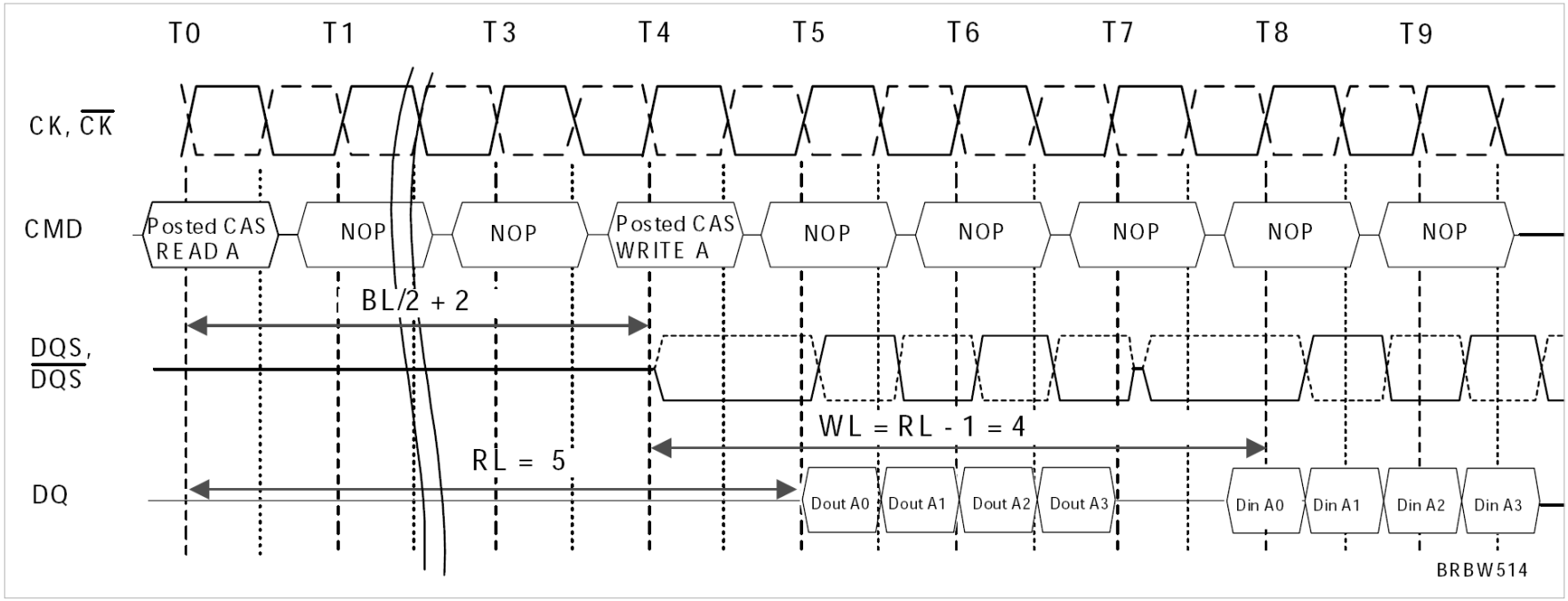
7. Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)



8. Burst Read Operation: RL = 3 (AL = 0, CL = 3, BL = 8)

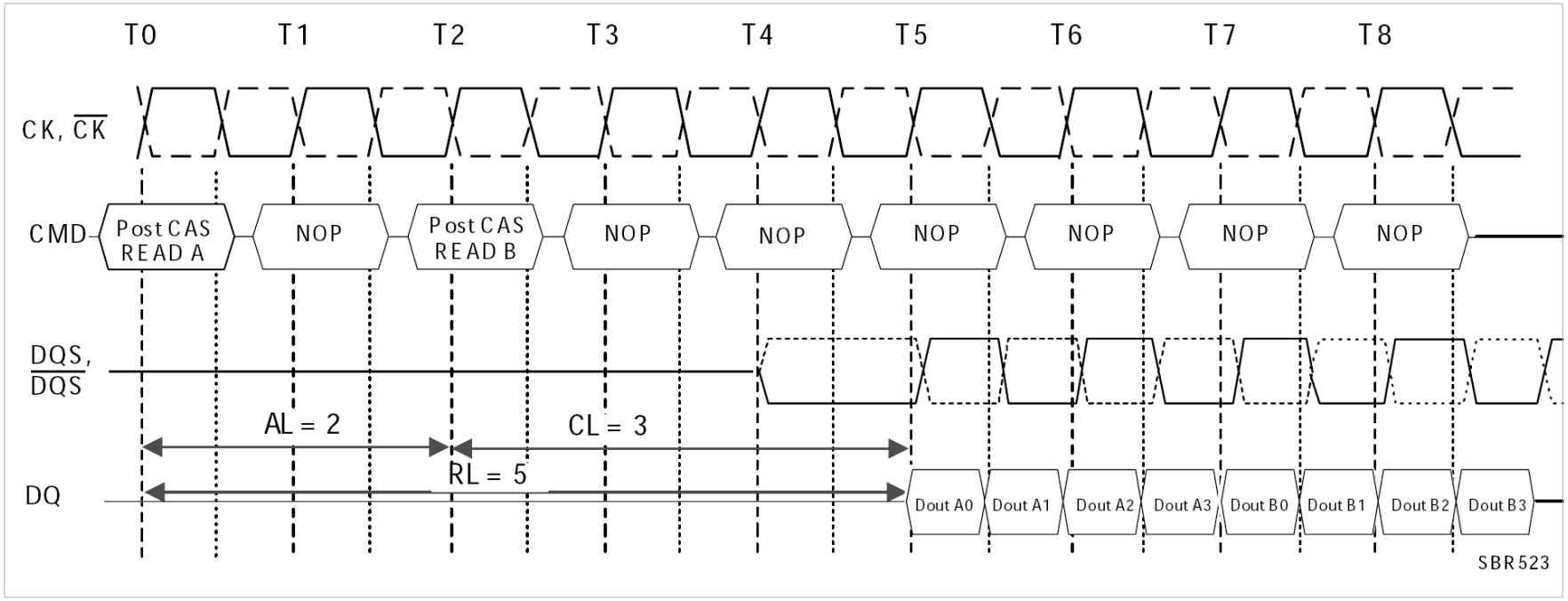


9. Burst Read followed by BurstWrite : RL = 5, WL = (RL-1) = 4, BL = 4

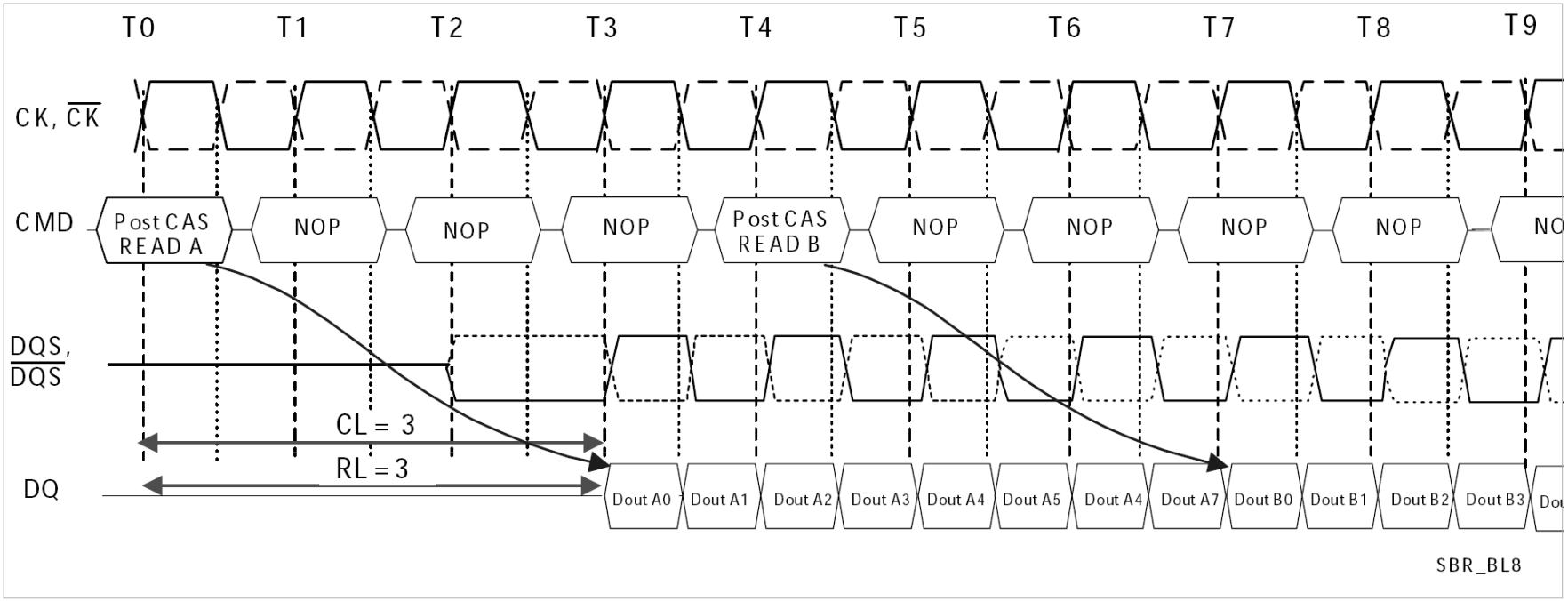


The minimum time from the burst read command to the burst write command is defined by a read-to-write turn-around time, which is BL/2 + 2 clocks.

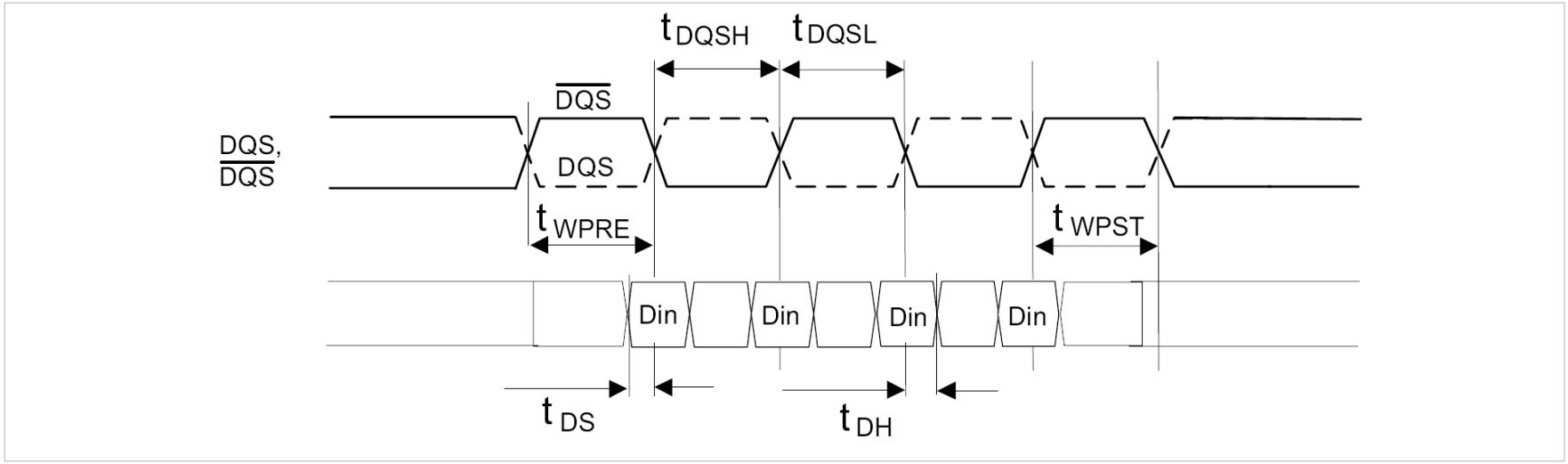
10. Seamless Burst Read Operation I: RL = 5, AL = 2, CL = 3, BL = 4



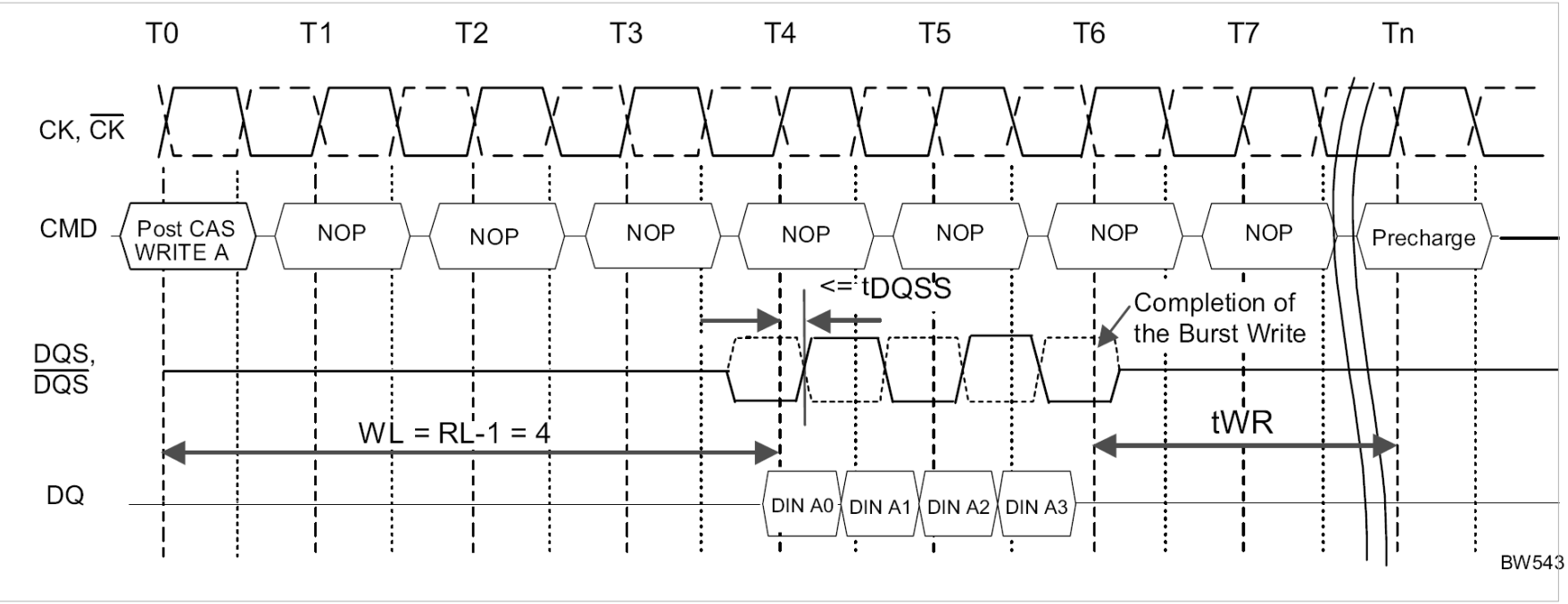
11. Seamless Burst Read Operation II: RL = 3, AL = 0, CL = 3, BL = 8 (non interrupting)



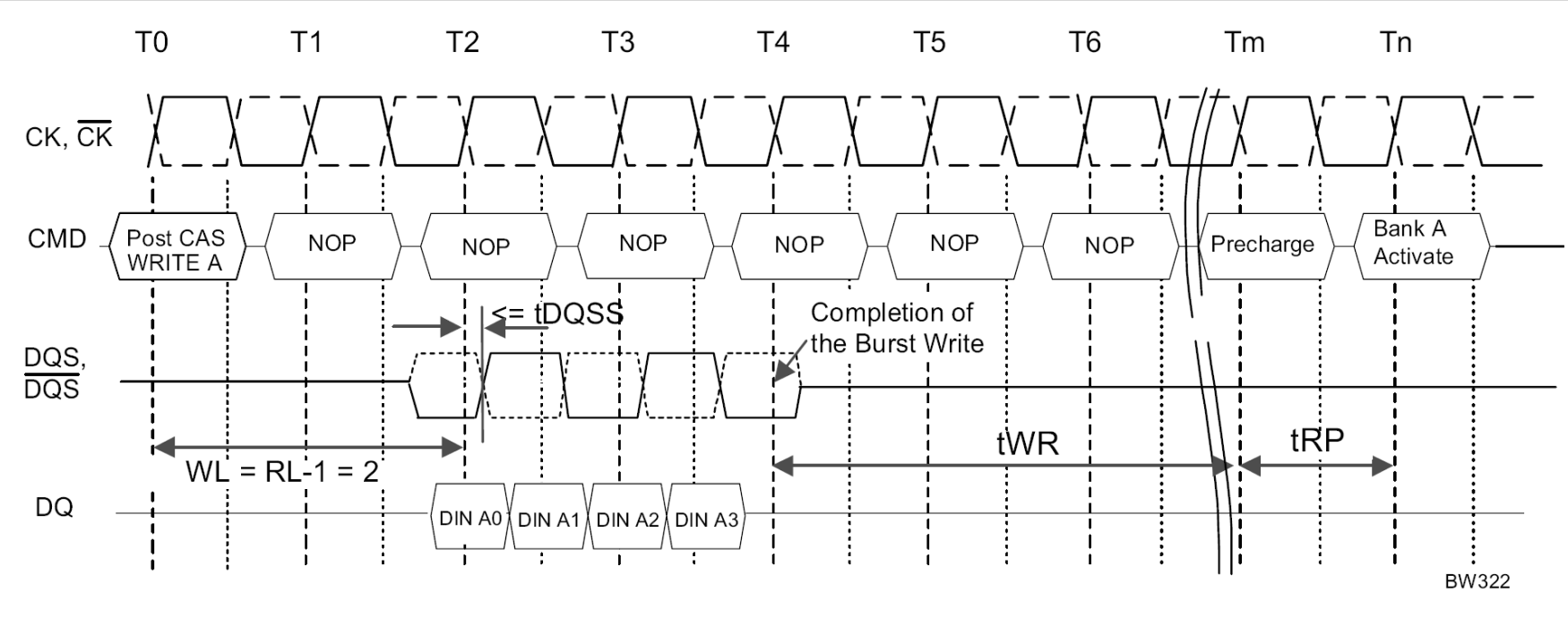
12. Basic Burst Write Timing



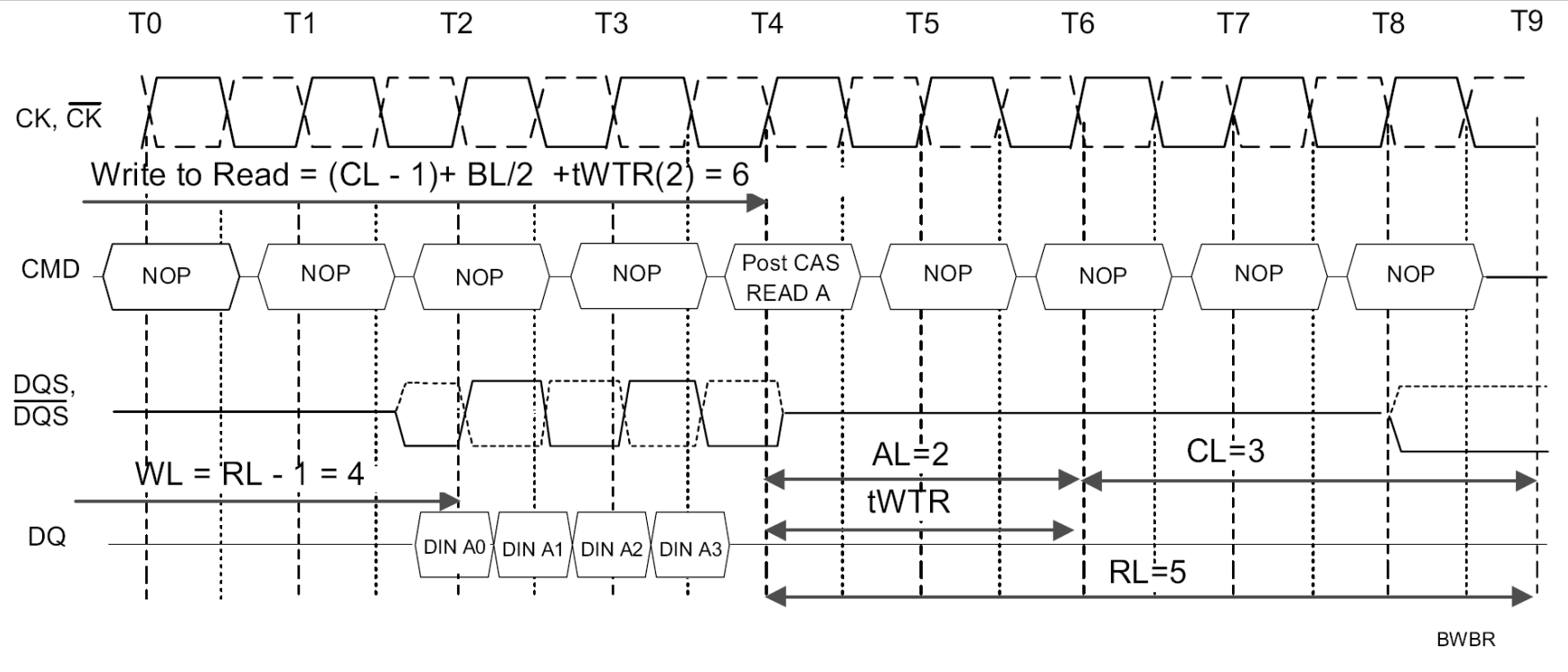
13. Burst Write Operation I: RL = 5 (AL = 2, CL = 3), WL = 4, BL = 4



14. Burst Write Operation II: RL = 3 (AL = 0, CL = 3), WL = 2, BL = 4

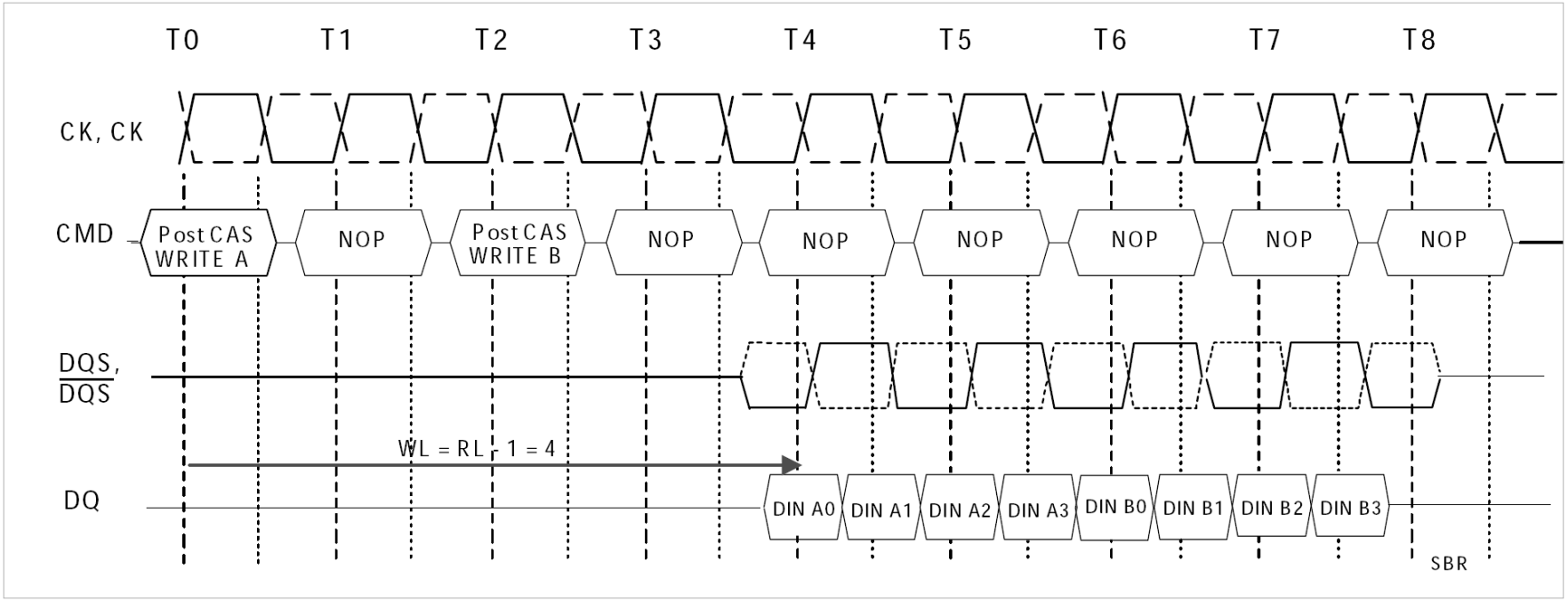


15. Burst Write followed by Burst Read: RL = 5 (AL = 2, CL = 3), WL = 4, tWTR = 2, BL = 4

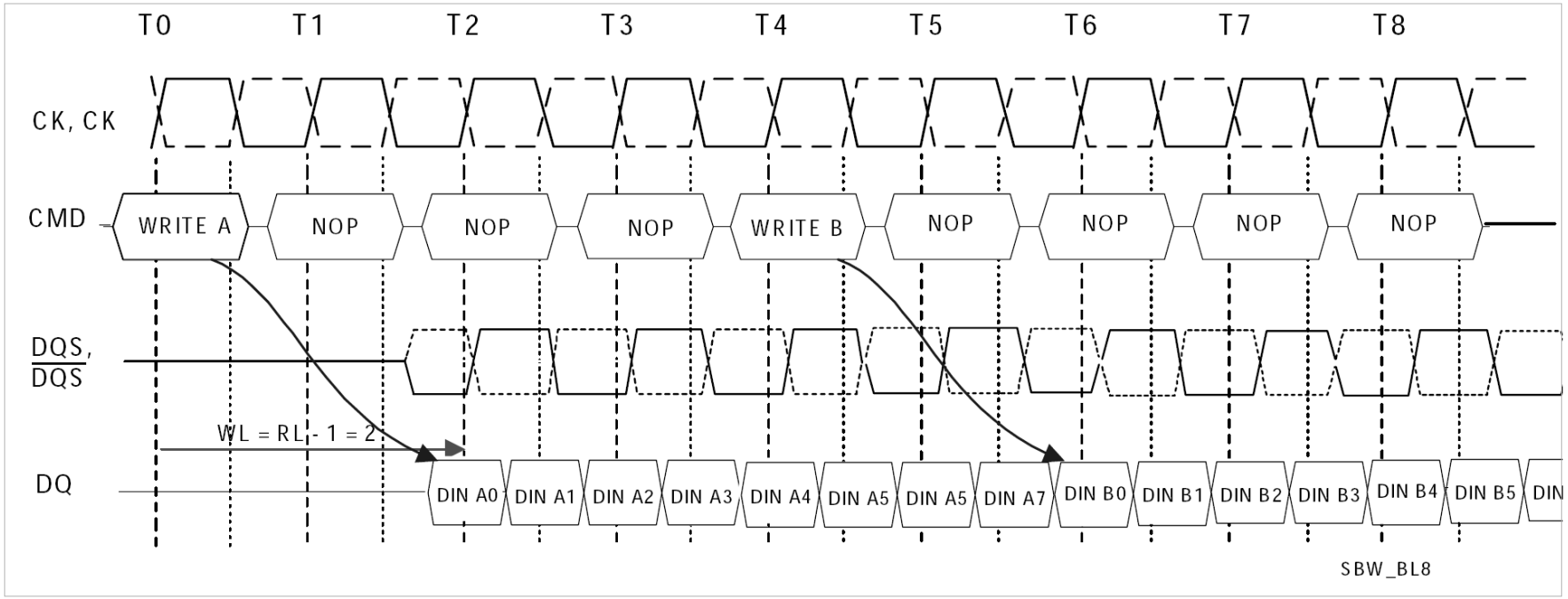


The minimum number of clocks from the burst write command to the burst read command is (CL - 1) +BL/2 + tWTR where tWTR is the write-to-read turn-around time tWTR expressed in clock cycles. The tWTR is not a write recovery time (tWR) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

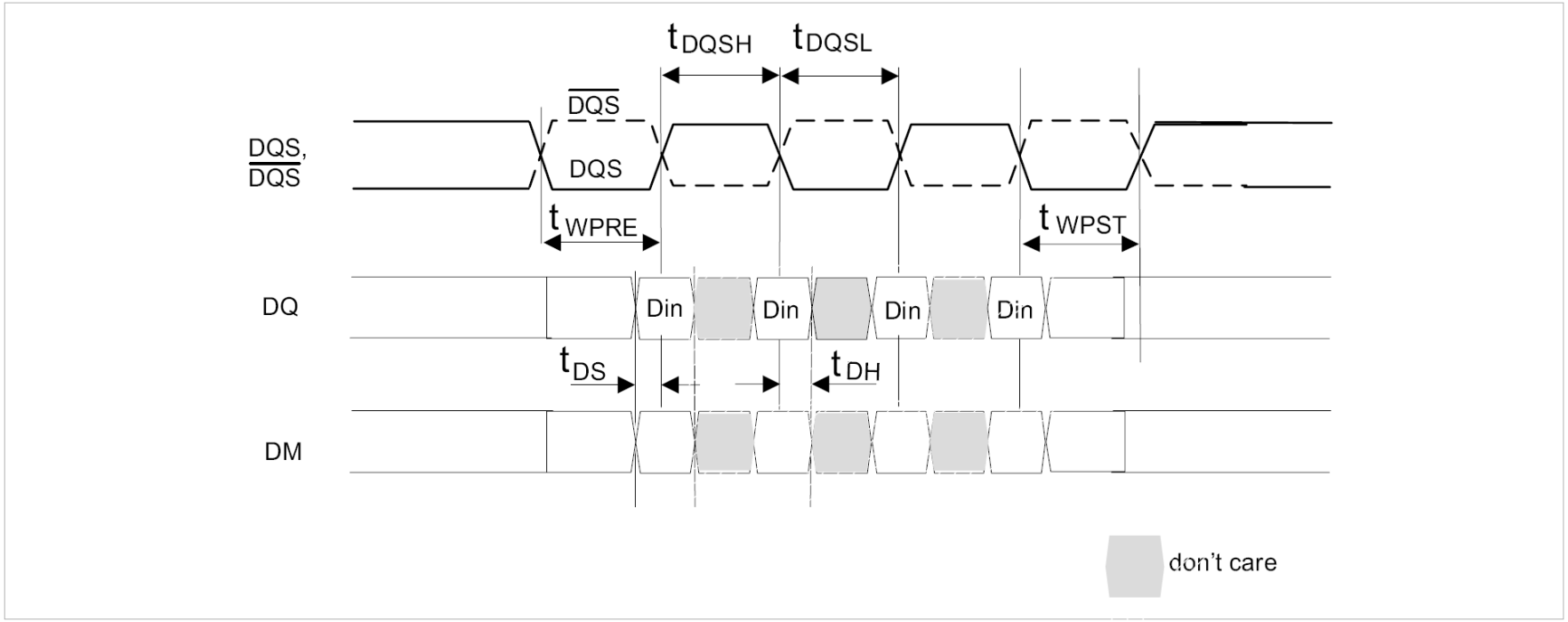
16. Seamless Burst Write Operation I: RL=5, WL=4, BL=4



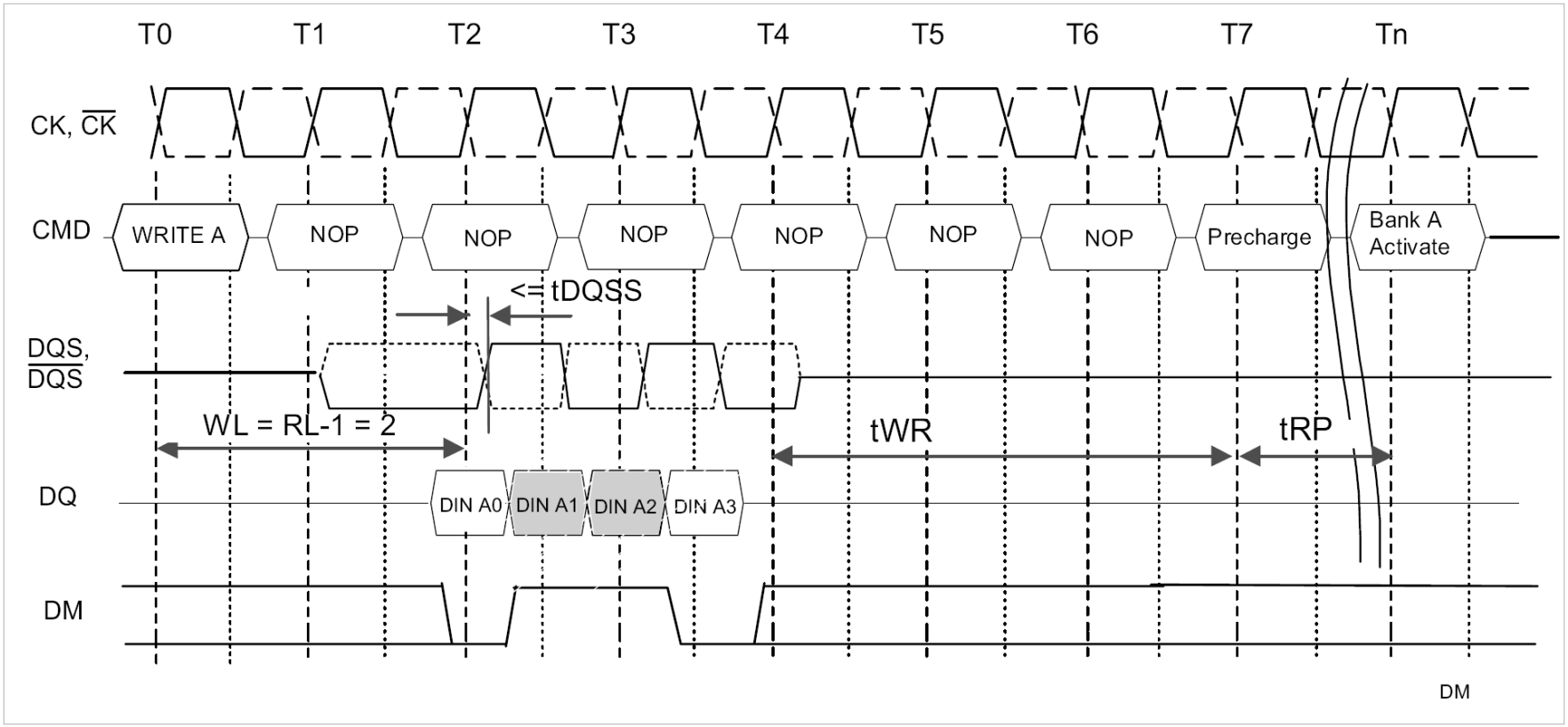
17. Seamless Burst Write Operation II: RL=3, WL=2, BL=8, non-interrupting



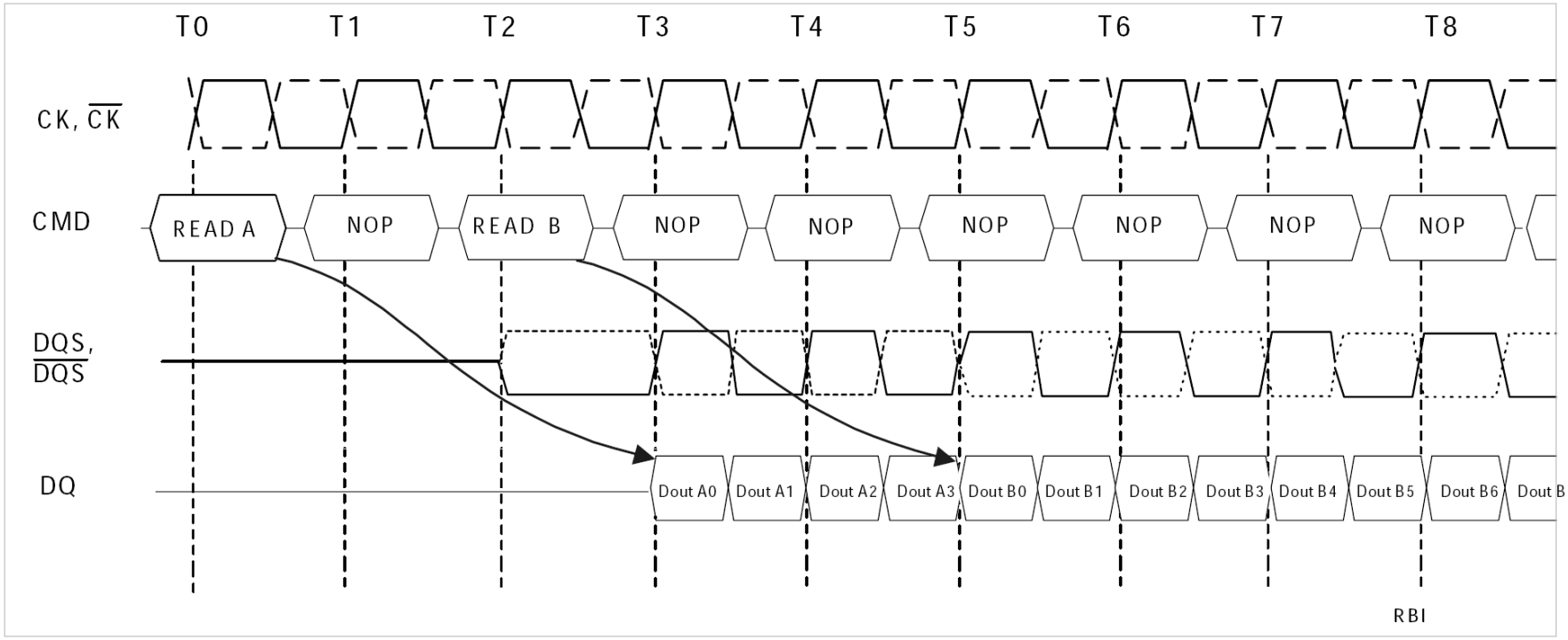
18. Write Data Mask Timing



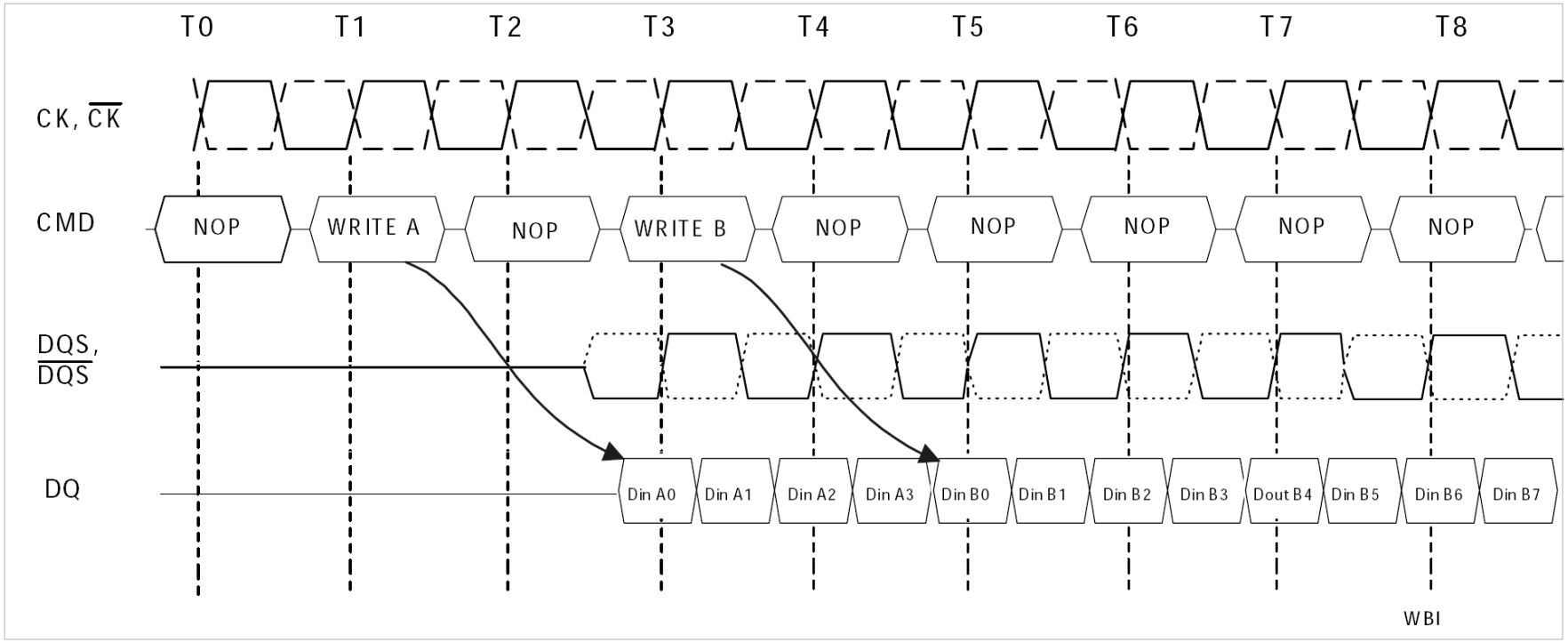
19. Burst Write Operation with Data Mask: RL = 3 (AL = 0, CL = 3), WL = 2, tWR = 3, BL = 4



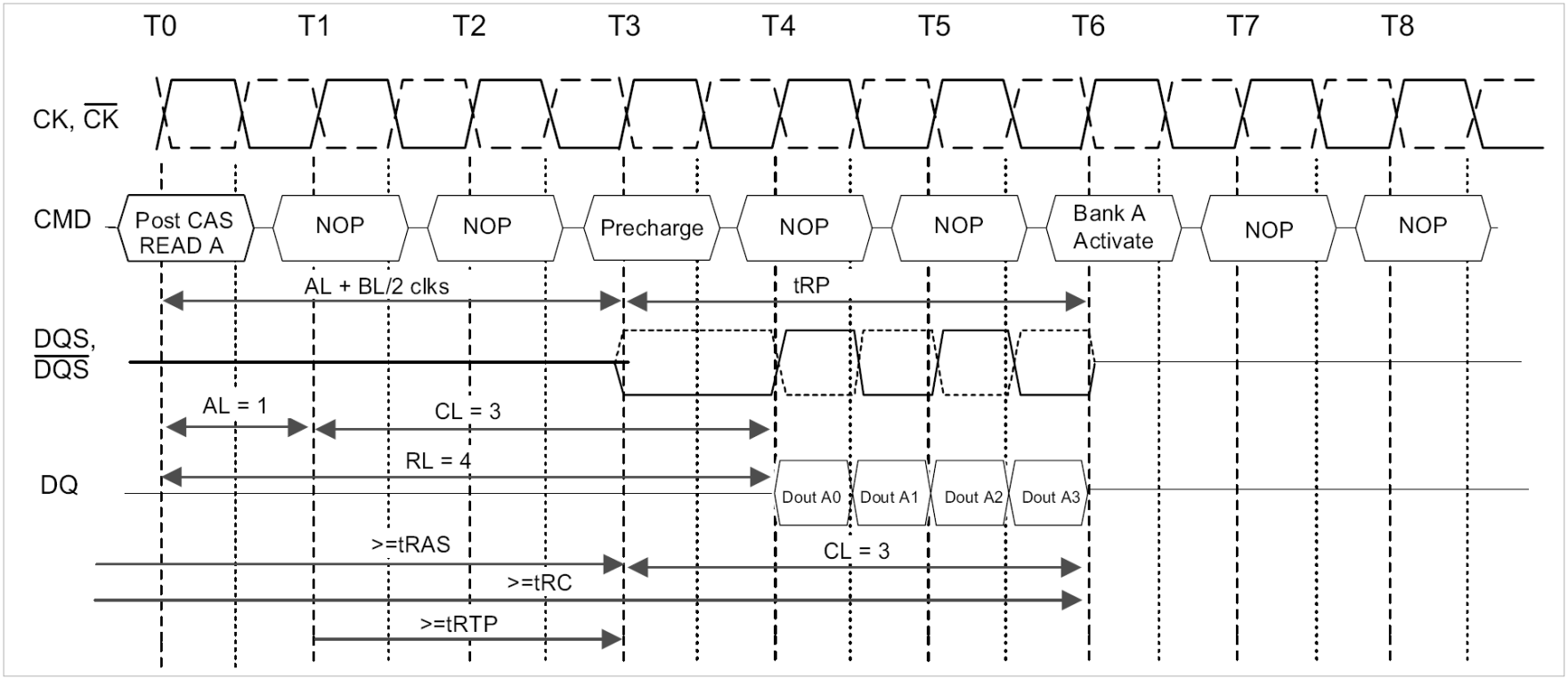
20. Read Burst Interrupt Timing: (CL = 3, AL = 0, RL = 3, BL = 8)



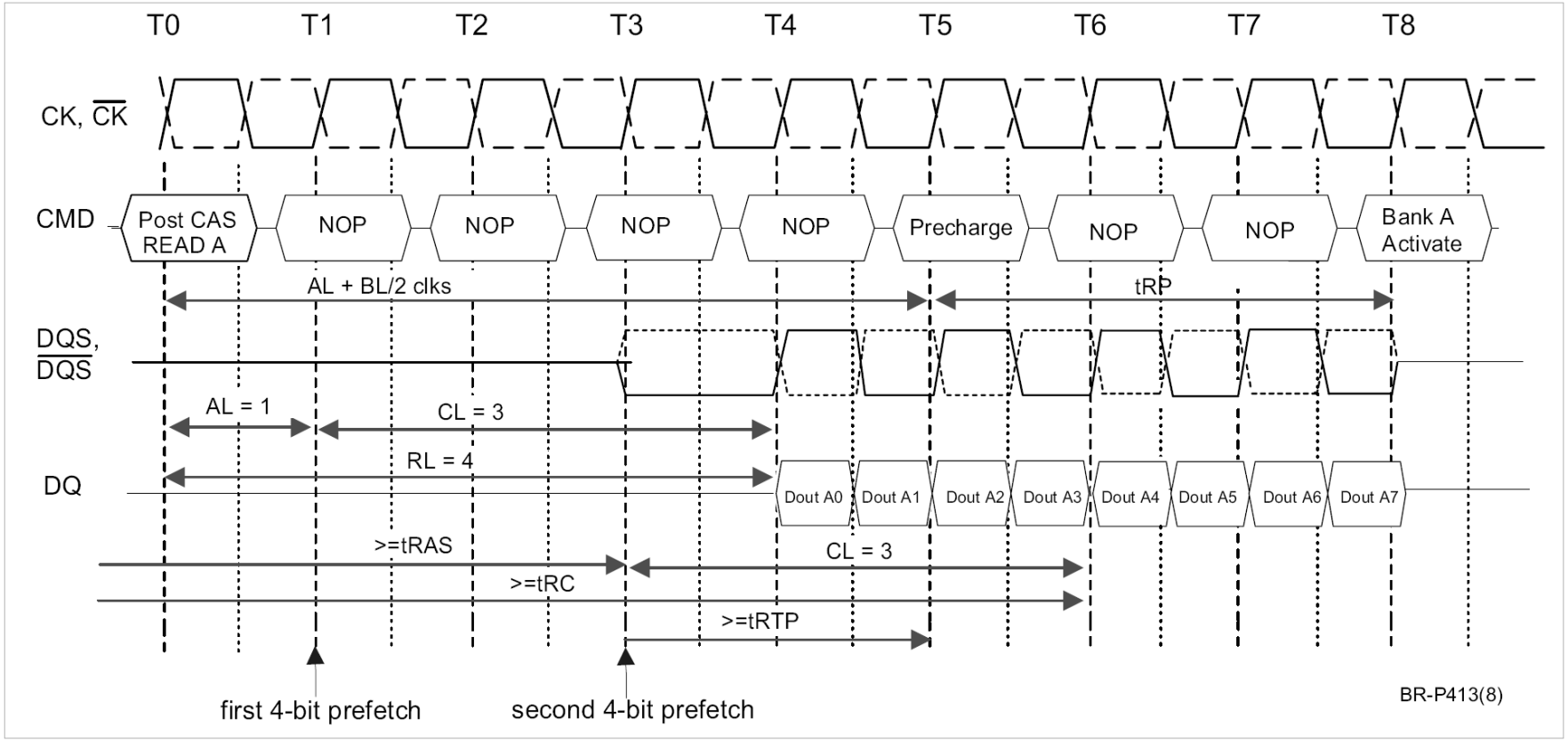
21. Write Burst Interrupt Timing: (C L = 3, AL = 0, WL = 2, BL = 8)



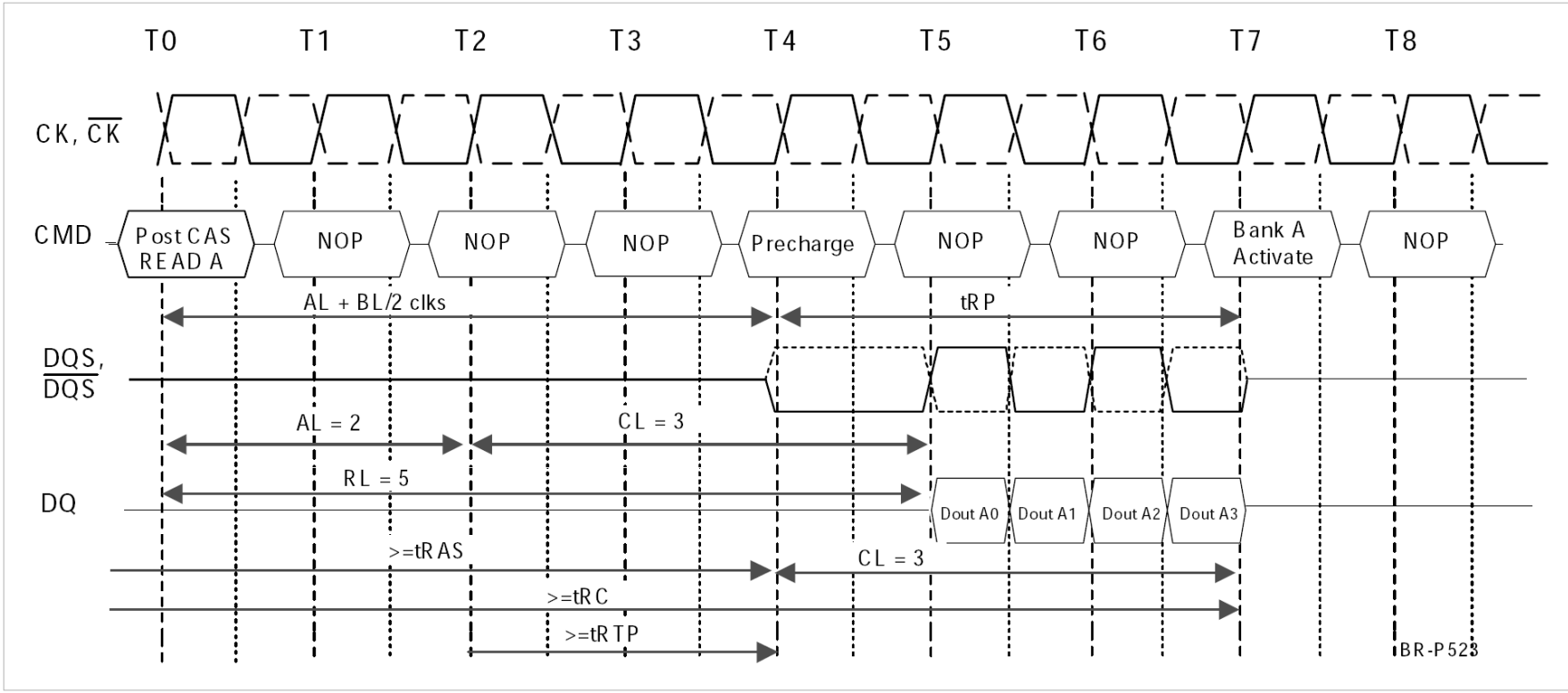
22. Burst Read Followed by Precharge I: RL = 4 (AL = 1, CL = 3), BL = 4, tRTP <= 2 clocks



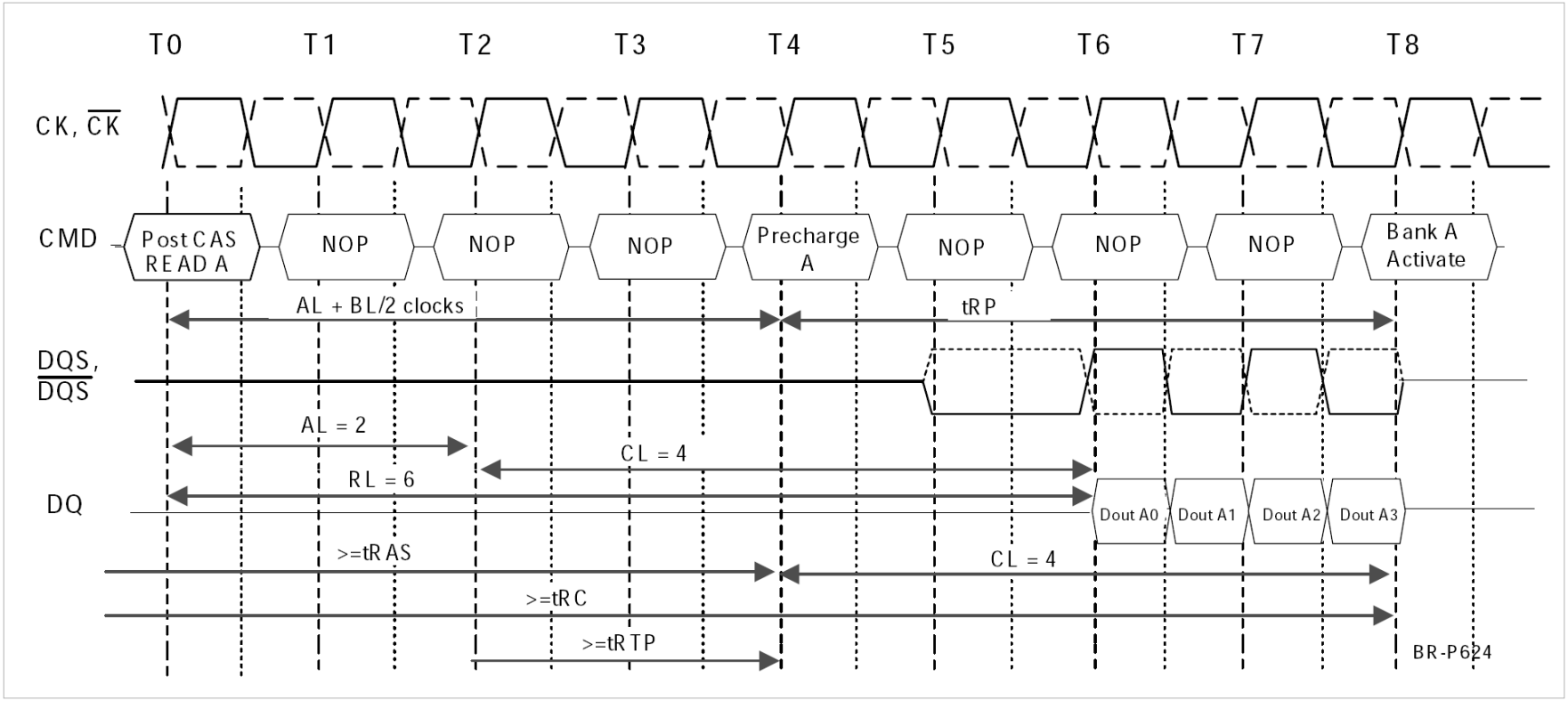
23. Burst Read Followed by Precharge II: RL = 4 (AL = 1, CL = 3), BL = 8, tRTP <= 2 clocks



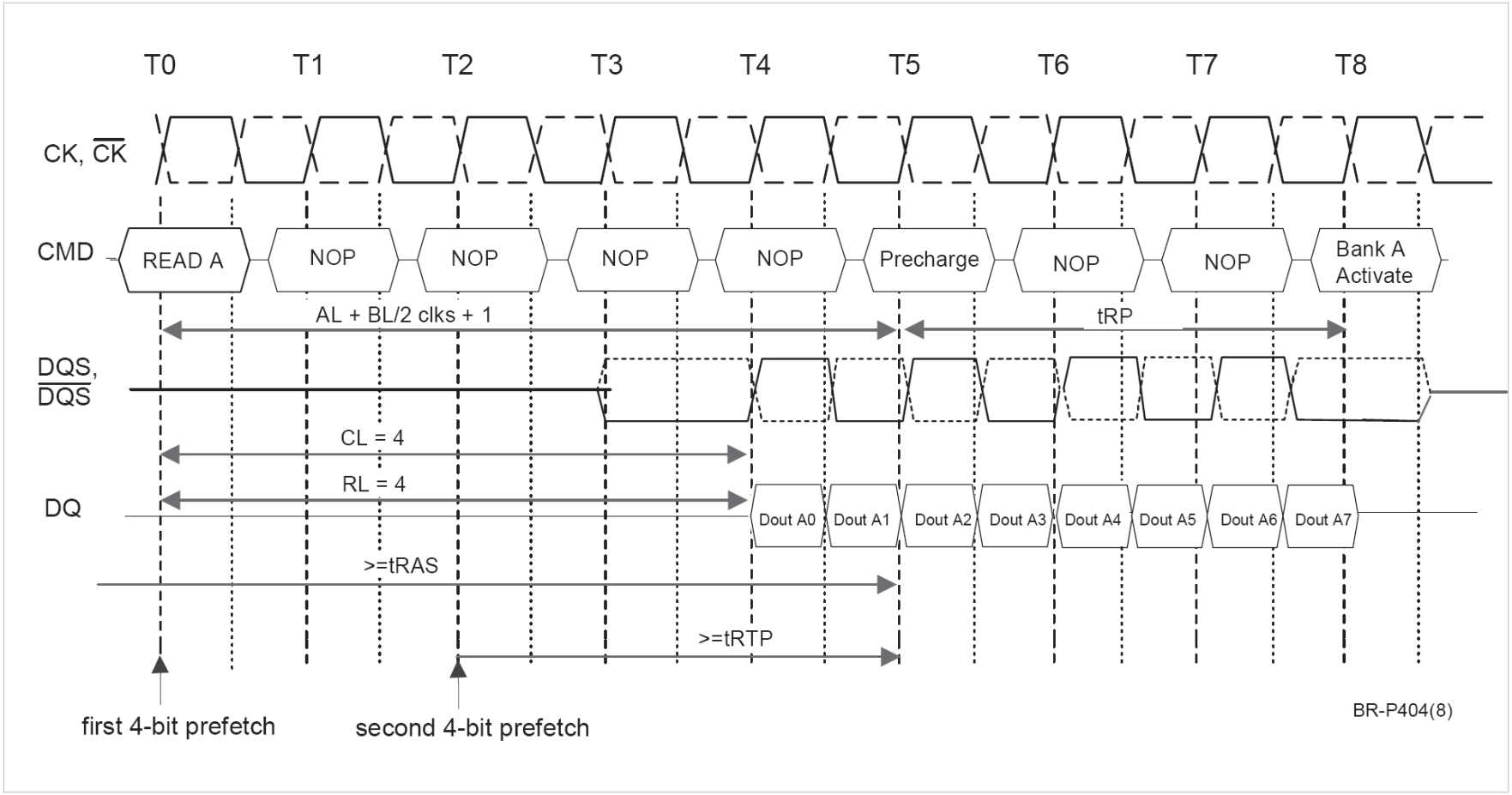
24. Burst Read Followed by Precharge III: RL=5(AL=2, CL=3), BL=4, tRTP<=2 clocks



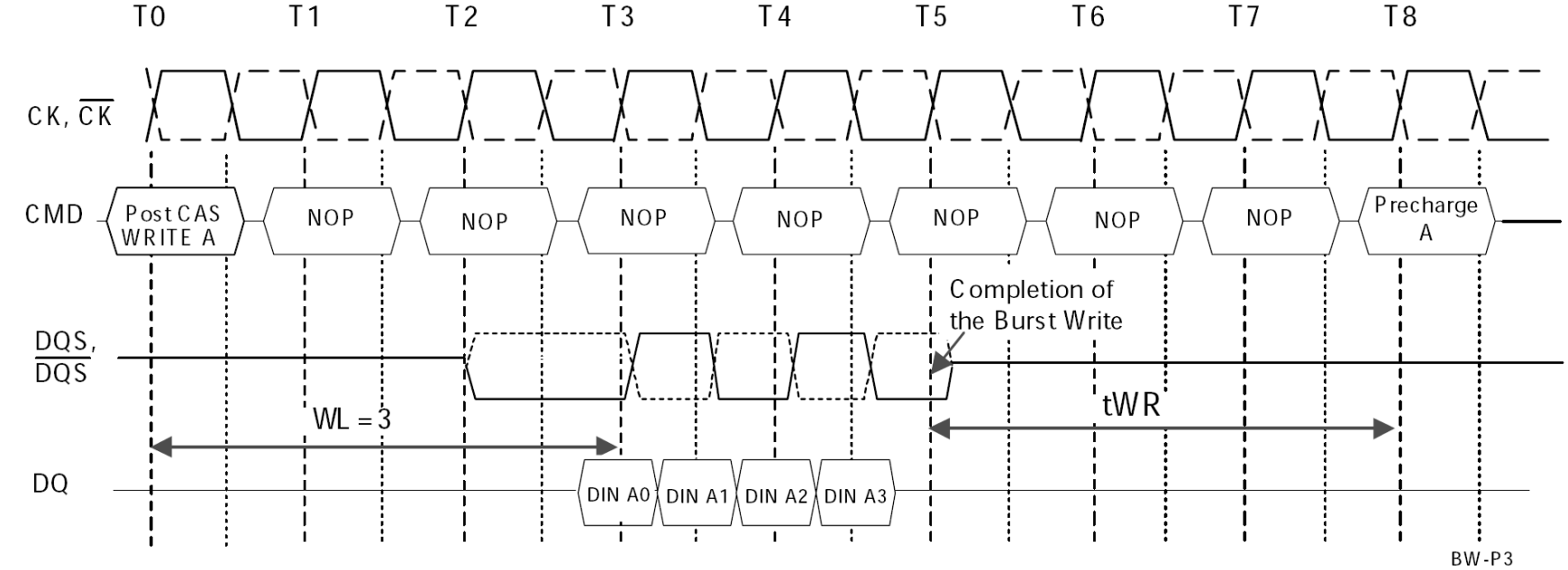
25. Burst Read Followed by Precharge IV: RL=6(AL=2, CL=4), BL=4, tRTP<=2 clocks



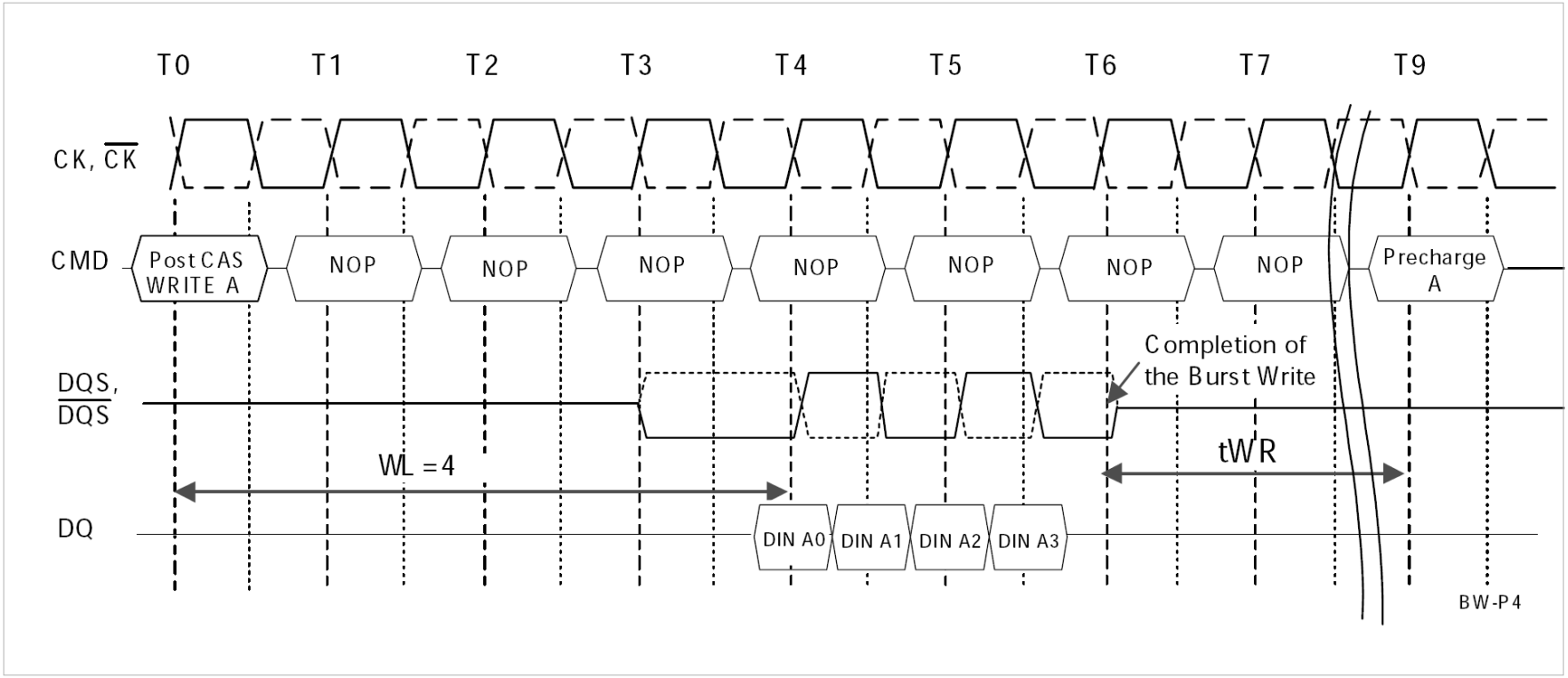
26. Burst Read Followed by Precharge V: RL=4, (AL=0, CL=4), BL=8, tRTP>2 clocks



27. Burst Write followed by Precharge I: WL = (RL - 1) = 3, BL = 4, tWR = 3

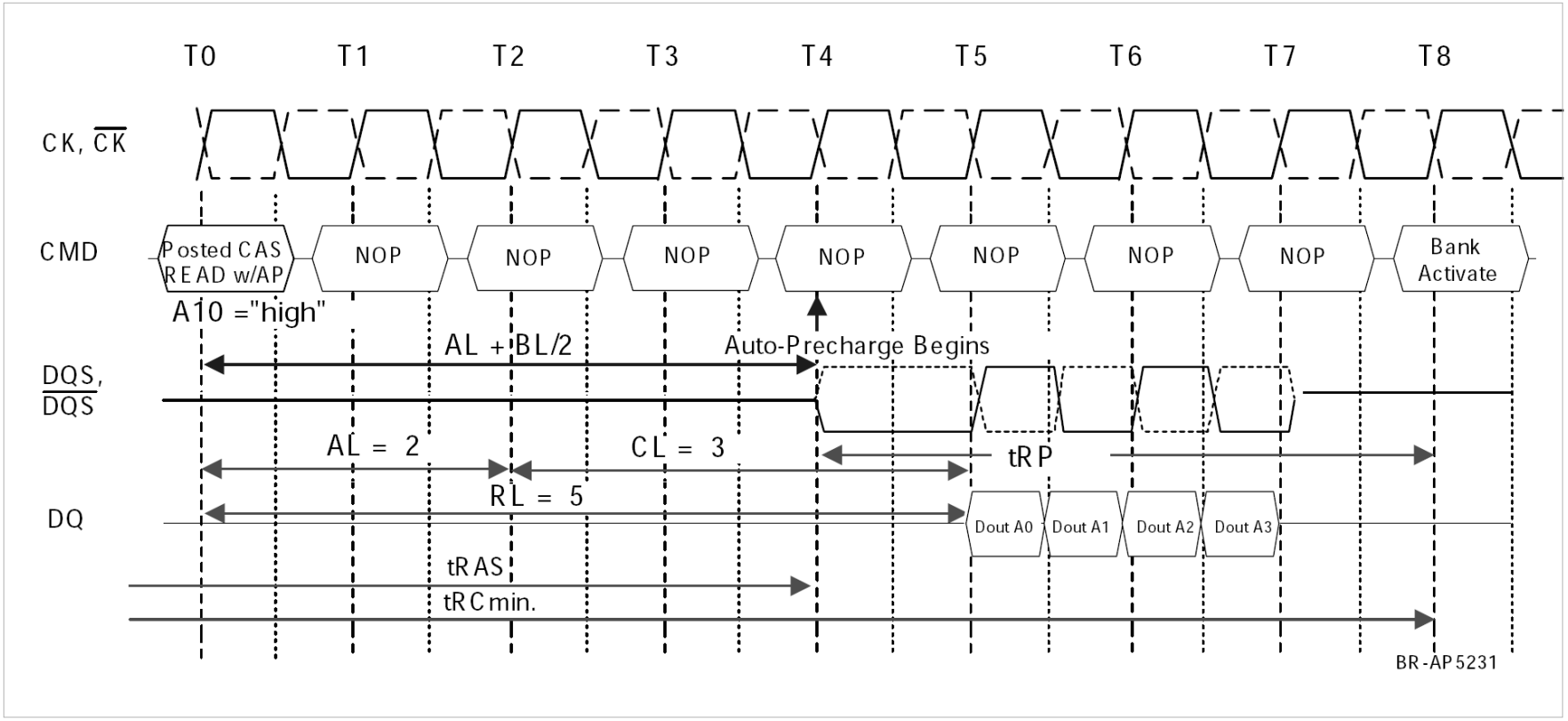


28. Burst Write followed by Precharge II: WL = (R L - 1) = 4, BL = 4, tWR = 3



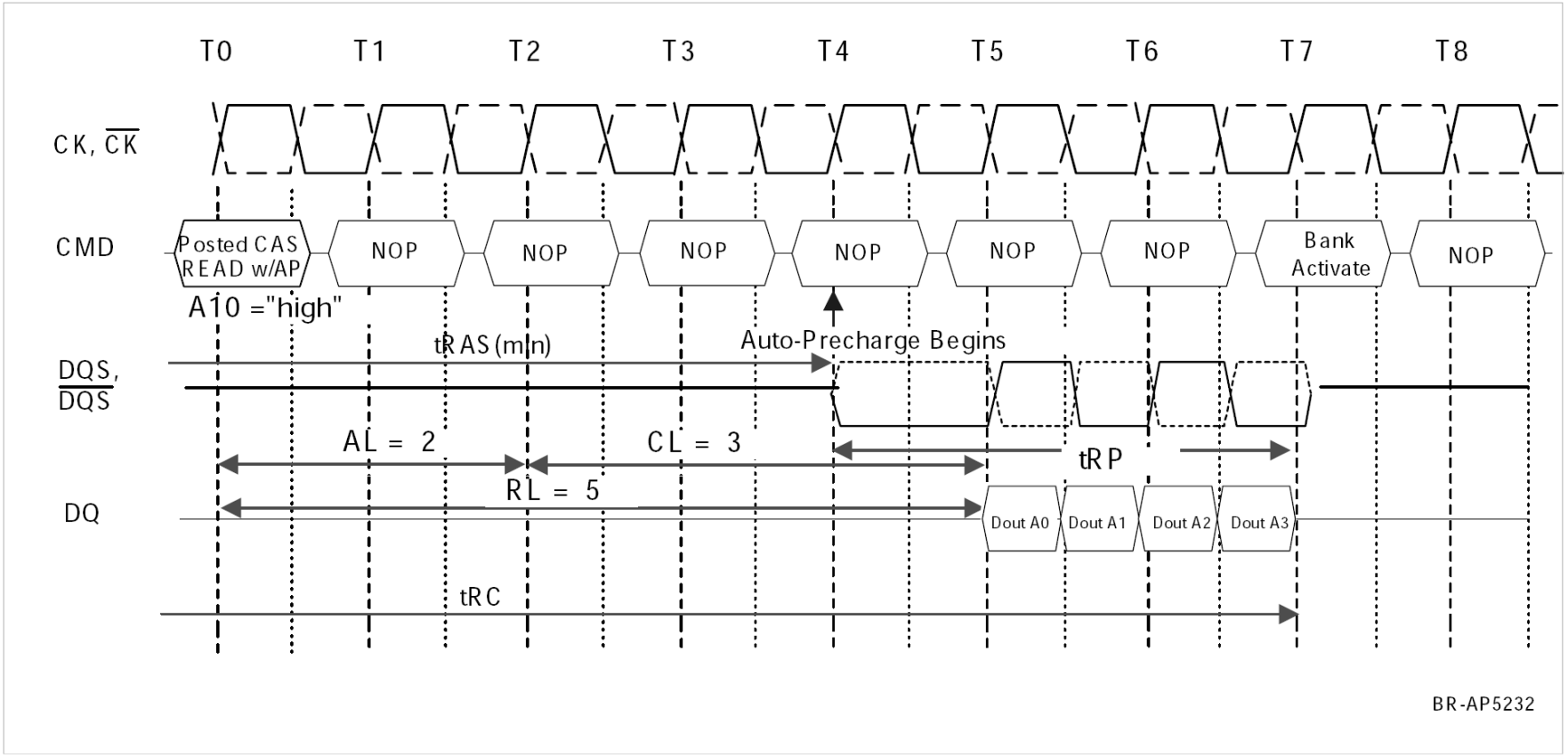
29. Burst Read with Auto-Precharge I: followed by an activation to the Same Bank (tRC Limit)

RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks



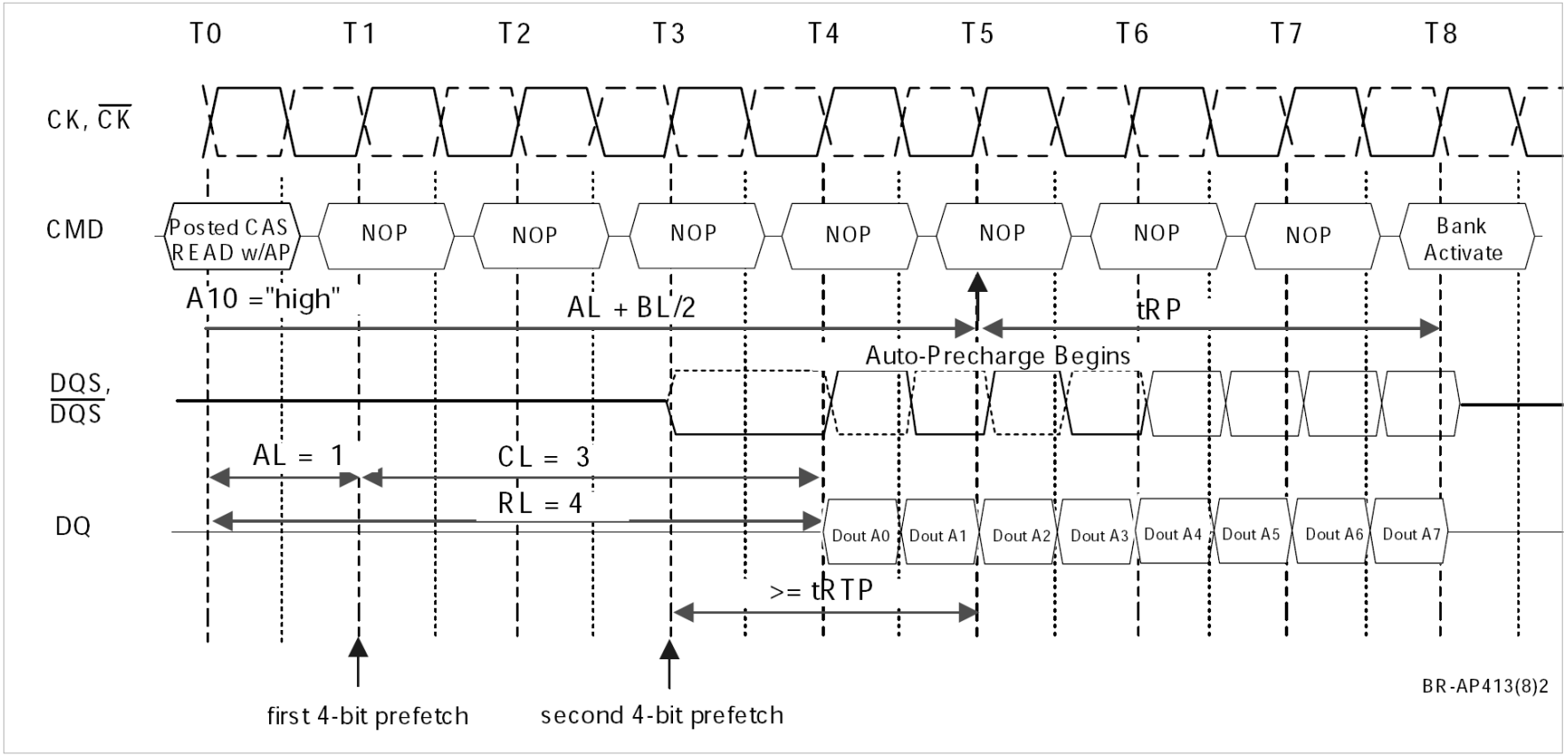
30. Burst Read with Auto-Precharge II: followed by an Activation to the Same Bank (tRAS Limit)

RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks



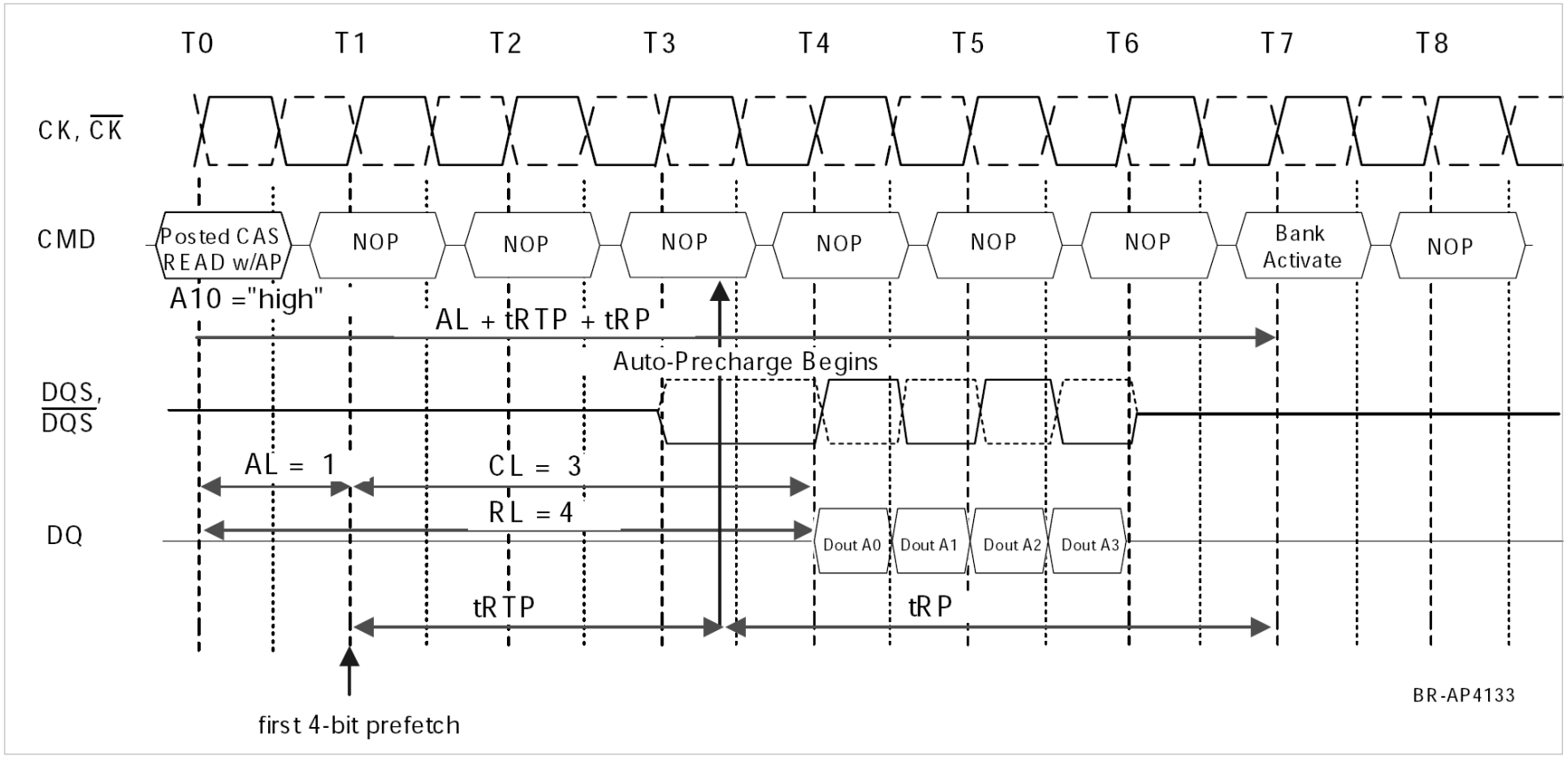
31. Burst Read with Auto-Precharge III: followed by an Activation to the Same Bank

RL=4(AL=1, CL=3), BL=8, tRTP<=2 clocks

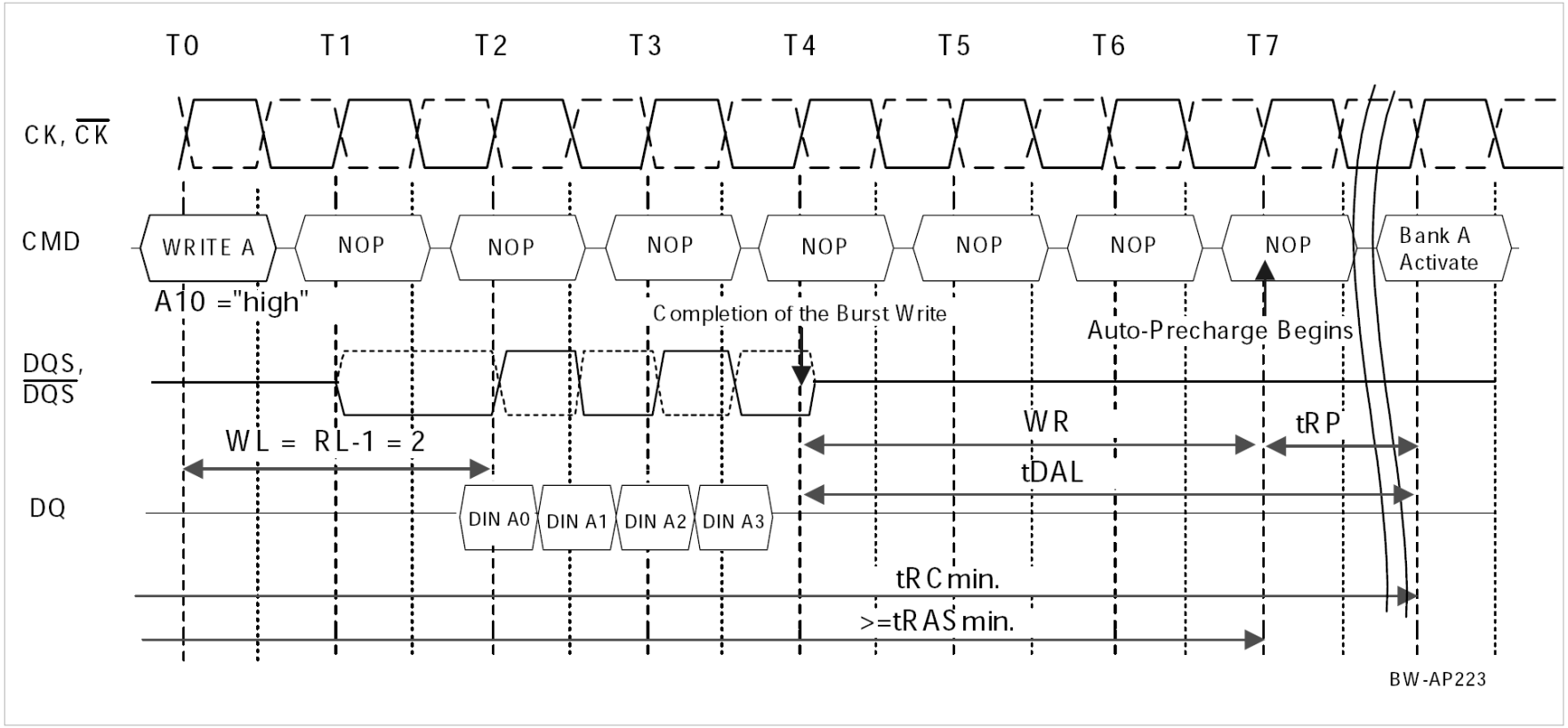


32. Burst Read with Auto-Precharge IV: followed by an Activation to the Same Bank

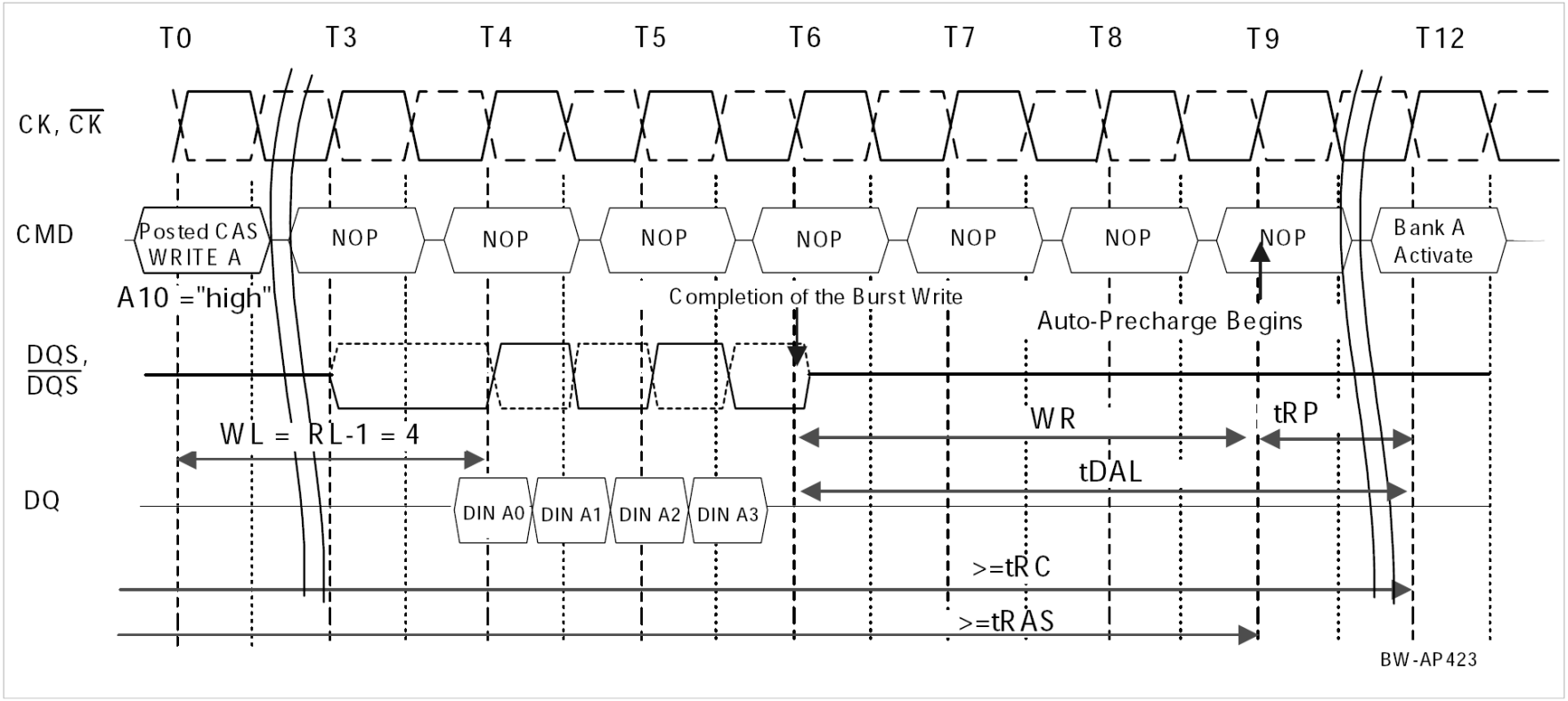
RL=4(AL=1, CL=3), BL=4, tRTP>2 clocks



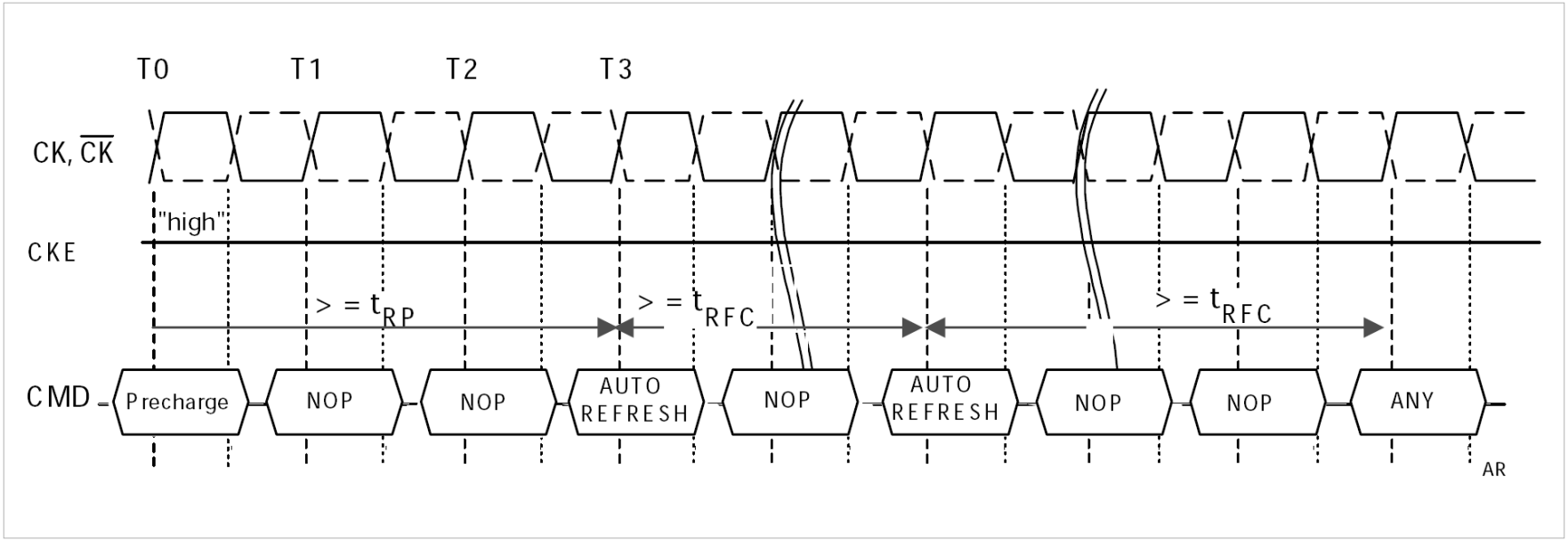
33. Burst Write with Auto-Precharge I: WL = 2, tDAL = 6 (WR = 3, tRP = 3), BL = 4 tRC Limit)



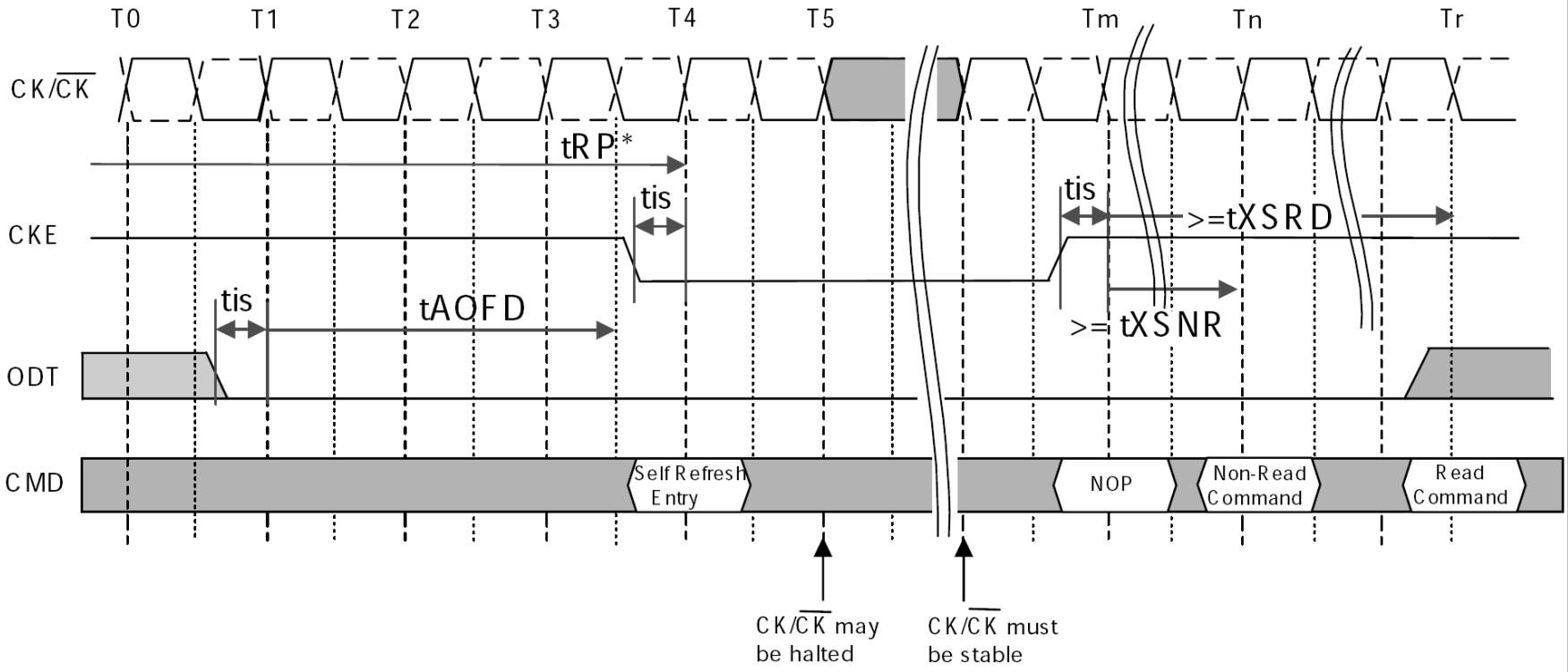
34. Burst Write with Auto-Precharge II: WL=4, tDAL=6(WR=3, tRP=3), BL=4 (WR+tRP Limit)



35. Auto-Refresh Command

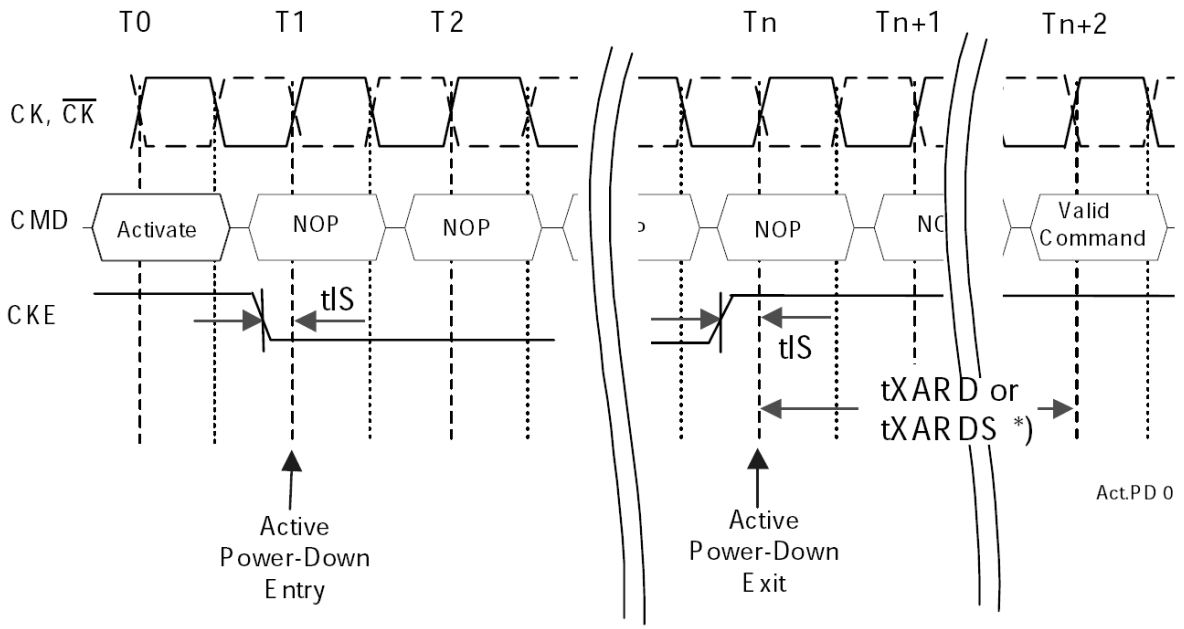


36. Self-Refresh Command



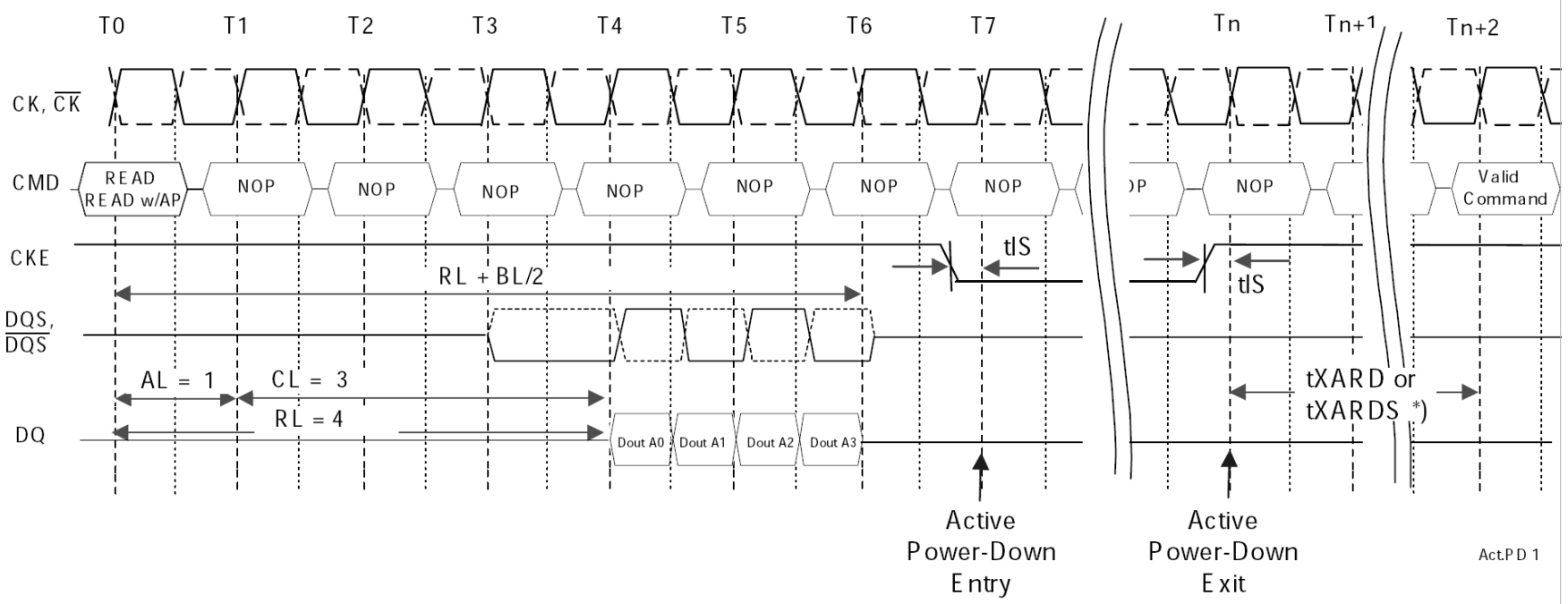
* = Device must be in the "All banks idle" state to entering Self Refresh mode.
ODT must be turned off prior to entering Self Refresh mode.
tXSRD has to be satisfied for a Read or a Read with Auto-Precharge command.
tXSNR has to be satisfied for any command except a Read or a Read with Auto-Precharge command.

37. Active Power-Down Mode Entry I: and Exit after an Activate Command



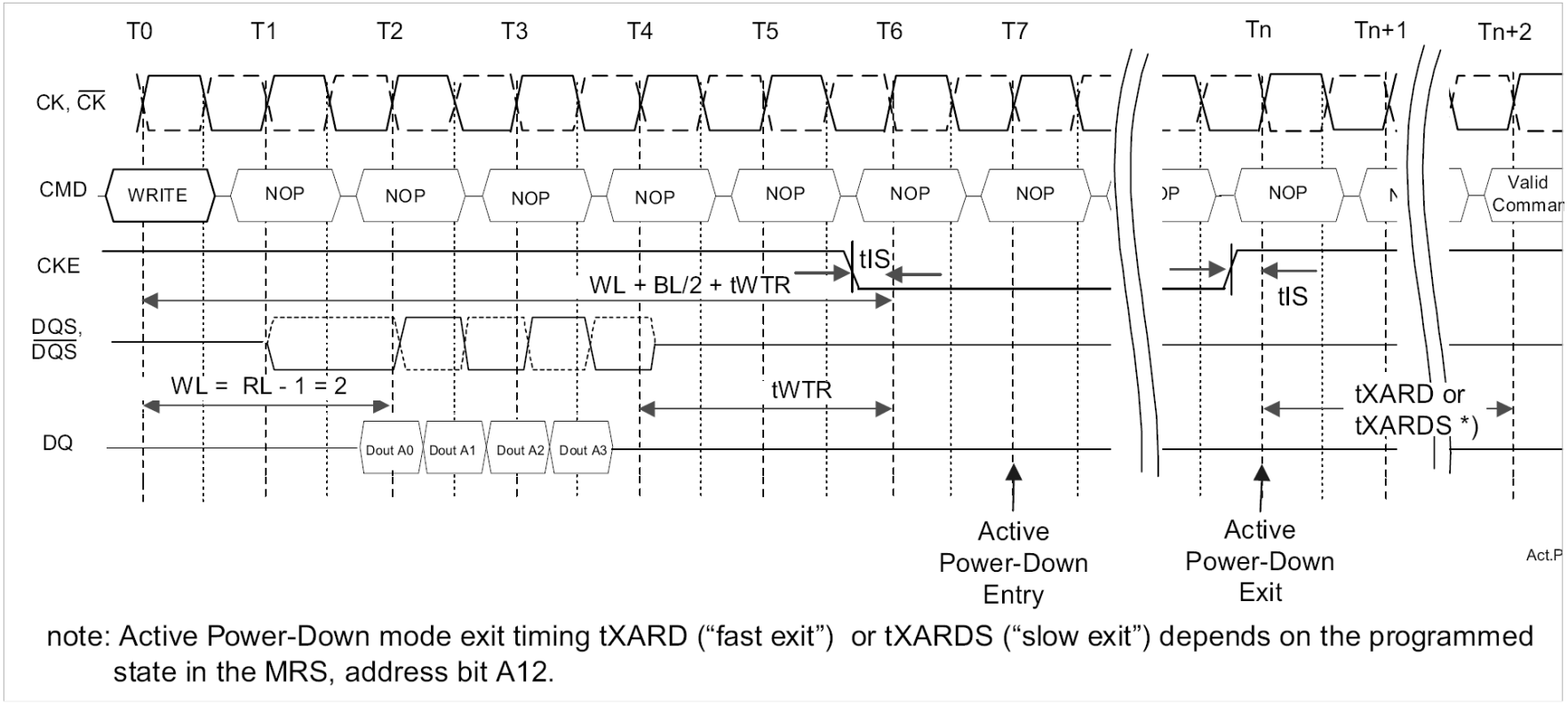
note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

38. Active Power-Down Mode Entry II: and Exit after a Read Burs t: R L = 4 (AL = 1, CL =3), BL = 4



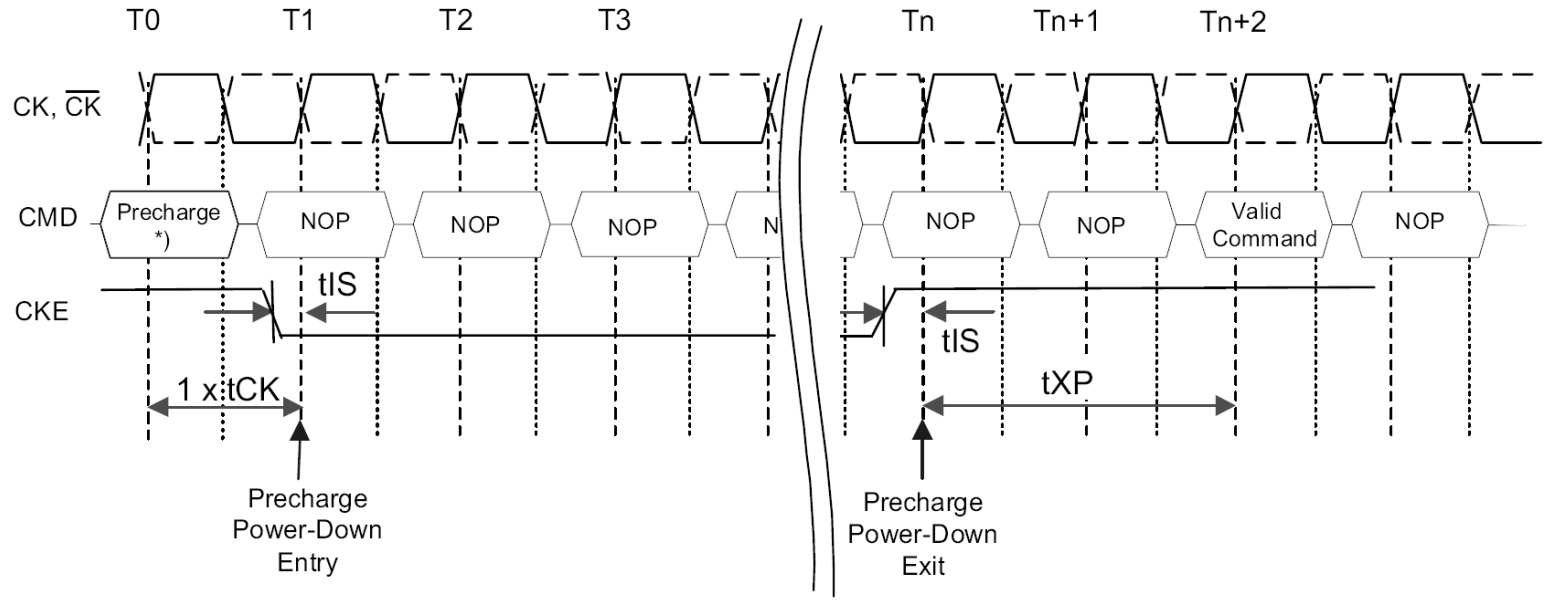
note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

39. Active Power-Down Mode Entry III: and Exit after a Write Burst: WL = 2, tWTR = 2, BL = 4



note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

40. Precharge Power Down Mode Entry and Exit



*) "Precharge" may be an external command or an internal precharge following Write with AP.

PrePD