Description

The EM47EM1688MBD is a 4Gb DDR3L SDRAM consisting of 32Mb x 8 banks x 16 bits I/O. DDR3L 1.35V is a low voltage version of DDR3 1.5V EM47EM1688SBD. The EM47EM1688MBD/SBD is packaged into 8x13 mm 96 Balls FBGA.

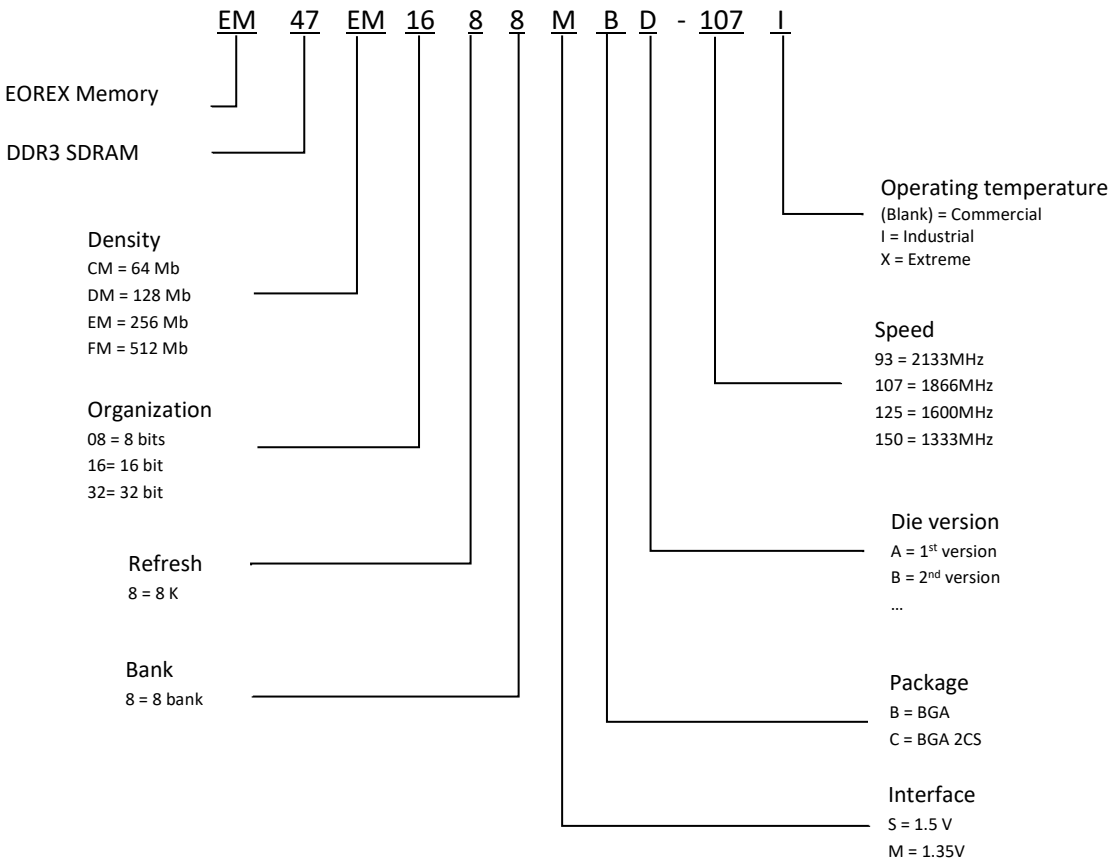
Features

- Power Supply: V_{DD} = 1.35V -0.065/+0.1V or 1.5V ± 0.075V
- V_{DDQ} = 1.35V -0.065/+0.1V or 1.5V ± 0.075V
- Functionality and operations comply with the DDR3/L SDRAM standards
- 8 internal banks
- 1 rank
- Speed: -125 is DDR3/L-1600, and -107 is DDR3/L-1866
- Data transfer rates: PC3-12800, and PC3-14900
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4 (Burst Chop)
- On-Die Termination (ODT)
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- This product is in compliance with the RoHS directive
- Operating temperature: -55°C to +125°C
  –64ms, 8192-cycle refresh at -55°C to +85°C
  –32ms at +85°C to +105°C
  –8ms at +105°C to +125°C

Revision History

Revision	Update
Revision 1.0 (Aug.2021)	First release
Revision 2.0 (Oct.2021)	Correct ball assignment.

Part Numbering



Ordering Information

Part No	Organization	Voltage	Max. Frequency	Package	Grade
EM47EM1688MBD-107	256M x 16	1.35V	DDR3L-1866 (13-13-13)	FBGA-96B	Commercial
EM47EM1688MBD-107I	256M x 16	1.35V	DDR3L-1866 (13-13-13)	FBGA-96B	Industrial
EM47EM1688MBD-107X	256M x 16	1.35V	DDR3L-1866 (13-13-13)	FBGA-96B	Extreme
EM47EM1688MBD-125	256M x 16	1.35V	DDR3L-1600 (11-11-11)	FBGA-96B	Commercial
EM47EM1688MBD-125I	256M x 16	1.35V	DDR3L-1600 (11-11-11)	FBGA-96B	Industrial
EM47EM1688MBD-125X	256M x 16	1.35V	DDR3L-1600 (11-11-11)	FBGA-96B	Extreme
EM47EM1688SBD-107	256M x 16	1.5V	DDR3-1866 (13-13-13)	FBGA-96B	Commercial
EM47EM1688SBD-107I	256M x 16	1.5V	DDR3-1866 (13-13-13)	FBGA-96B	Industrial
EM47EM1688SBD-107X	256M x 16	1.5V	DDR3-1866 (13-13-13)	FBGA-96B	Extreme
EM47EM1688SBD-125	256M x 16	1.5V	DDR3-1600 (11-11-11)	FBGA-96B	Commercial
EM47EM1688SBD-125I	256M x 16	1.5V	DDR3-1600 (11-11-11)	FBGA-96B	Industrial
EM47EM1688SBD-125X	256M x 16	1.5V	DDR3-1600 (11-11-11)	FBGA-96B	Extreme

Note: Speed (^{t}CK*) is in order of CL-^{t}RCD-^{t}RP

Ball Assignment

Top view						
1	2	3		7	8	9
VDDQ	DQ13	DQ15	A	DQ12	VDDQ	VSS
VSSQ	VDD	VSS	B	/UDQS	DQ14	VSSQ
VDDQ	DQ11	DQ9	C	UDQS	DQ10	VDDQ
VSSQ	VDDQ	UDM	D	DQ8	VSSQ	VDD
VSS	VSSQ	DQ0	E	LDM	VSSQ	VDDQ
VDDQ	DQ2	LDQS	F	DQ1	DQ3	VSSQ
VSSQ	DQ6	/LDQS	G	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4	H	DQ7	DQ5	VDDQ
NC	VSS	/RAS	J	CK	VSS	NC
ODT	VDD	/CAS	K	/CK	VDD	CKE
NC	/CS	/WE	L	A10/AP	ZQ	NC
VSS	BA0	BA2	M	NC	VREFCA	VSS
VDD	A3	A0	N	A12/BC	BA1	VDD
VSS	A5	A2	P	A1	A4	VSS
VDD	A7	A9	R	A11	A6	VDD
VSS	/RESET	A13	T	A14	A8	VSS

Ball Description

Symbol	Type	Function
CK, /CK	Input	**Clock:** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Pre-charge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self- refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self Refresh.
/CS	Input	**Chip Select:** All commands are masked when /CS is registered HIGH. /CS provides for external Rank selection on systems with multiple Ranks. /CS is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3/L SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS and DM. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT.
/RAS, /CAS, /WE	Input	**Command Inputs:** /RAS, /CAS and /WE (along with /CS) define the command being entered.
UDM, LDM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0~ BA2	Input	**Bank Address Inputs:** BA0-BA2 define the bank to which an Active, Read, Write or Pre-charge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0~ A14	Input	**Address Inputs:** Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during Mode Register Set commands. (A10/AP and A12/BC have additional functions, see below)
A10 / AP	Input	**Auto Pre-charge:** A10 is sampled during Read/Write commands to determine whether Auto pre-charge should be performed to the accessed bank after the Read/Write operation (HIGH: Auto pre-charge; LOW: No Auto pre-charge). A10 is sampled during a Pre-charge command to determine whether the Pre-charge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be pre-charged, the bank is selected by bank addresses.
A12 / BC	Input	**Burst Chop:** A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.

Symbol	Type	Function
/RESET	Input	**Input Reset**: /RESET is an active LOW CMOS input referenced to V_{SS}. The /RESET input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. /RESET assertion and desertion are asynchronous.
DQ0~ DQ15	I/O	**Data Input/ Output:** Bi-directional data bus.
UDQS, /UDQS LDQS, /LDQS	I/O	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR3/L SDRAM supports differential data strobe only and does not support single-ended.
V_{DDQ}	Supply	**DQ Power Supply:** 1.35V - 0.065/+0.1V or 1.5V +/- 0.075V
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 1.35V -0.065/+0.1V or 1.5V +/- 0.075V
V_{SS}	Supply	**Ground**
V_{REFDQ}	Reference	**Reference voltage for DQ Pins**
V_{REFCA}	Reference	**Reference voltage for Command, Control, and Address Pins**
ZQ	Reference	**Reference Pin for ZQ calibration:** series 240Ω resistor to V_{SS}
NC	-	**Not Connected Internally.**
Note: Input only pins (BA0-BA2, A0-A15, /RAS, /CAS, /WE, /CS, CKE, ODT and /RESET) do not supply termination.		

Absolute Maximum Rating

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.4 ~ +1.975		V
V_{DD}	Power Supply Voltage	-0.4 ~ +1.975		V
V_{DDQ}	Power Supply Voltage	-0.4 ~ +1.975		V
T_{OP}	Operating Temperature Range	Commercial	0~ +95	°C
		Industrial	-40~ +95	°C
		Extreme	-55~ +125	°C
T_{STG}	Storage Temperature Range	-55 ~ +125		°C
V_{REFCA}	Reference Voltage for Control	-0.4 ~ 0.6 × V_{DD}		V
V_{REFDQ}	Reference Voltage for DQ	-0.4 ~ 0.6 × V_{DDQ}		V

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

Recommended DC Operating Conditions

(V_{DD}, V_{DDQ} = 1.35V -0.065/+0.1V)

Symbol	Parameter & Test Conditions	-107	-125	Units
		Max		
IDD_1	**Operating One Bank Active-Read-Pre-charge Current:** CKE: High; External clock: On; t_{CK}, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	46	45	mA
IDD_{2P1}	**Pre-charge Power-Down Current Fast Exit:** CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0;/CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	12	12	mA
IDD_{2N}	**Pre-charge Standby Current:** CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0;/CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	17	17	mA
IDD_{3P}	**Active Power-Down Current:** CKE: Low; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0;/CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	17	17	mA
IDD_{4W}	**Operating Burst Write Current:** CKE: High; External clock: On; t_{CK}, CL: see timing used table; BL: 8; AL: 0;/CS: High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	130	125	mA

Symbol	Parameter & Test Conditions	-107	-125	Units
IDD_{5B}	**Burst Refresh Current:** CKE: High; External clock: On; t_{CK}, CL, nRFC: see timing used table; BL: 8; AL: 0; /CS: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	156	152	mA
IDD_6	**Self-Refresh Current: Normal Temperature Range;** T_C: 0- 85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and /CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	15	15	mA
IDD_{6_RS}		15	15	mA
IDD_7	**Operating Bank Interleave Read Current;** CKE: High; External clock: On; t_{CK}, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	147	140	mA

Note 1: Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

Note 2: Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5, 1] = 01B; RTT_Nom enable: set MR1 A[9, 6, 2] = 011B; RTT_Wr enable: set MR2 A[10, 9] = 10B

Note 3: Pre-charge Power Down Mode: set MR0 A12 = 0B for Slow Exit or MR0 A12 = 1B for Fast Exit

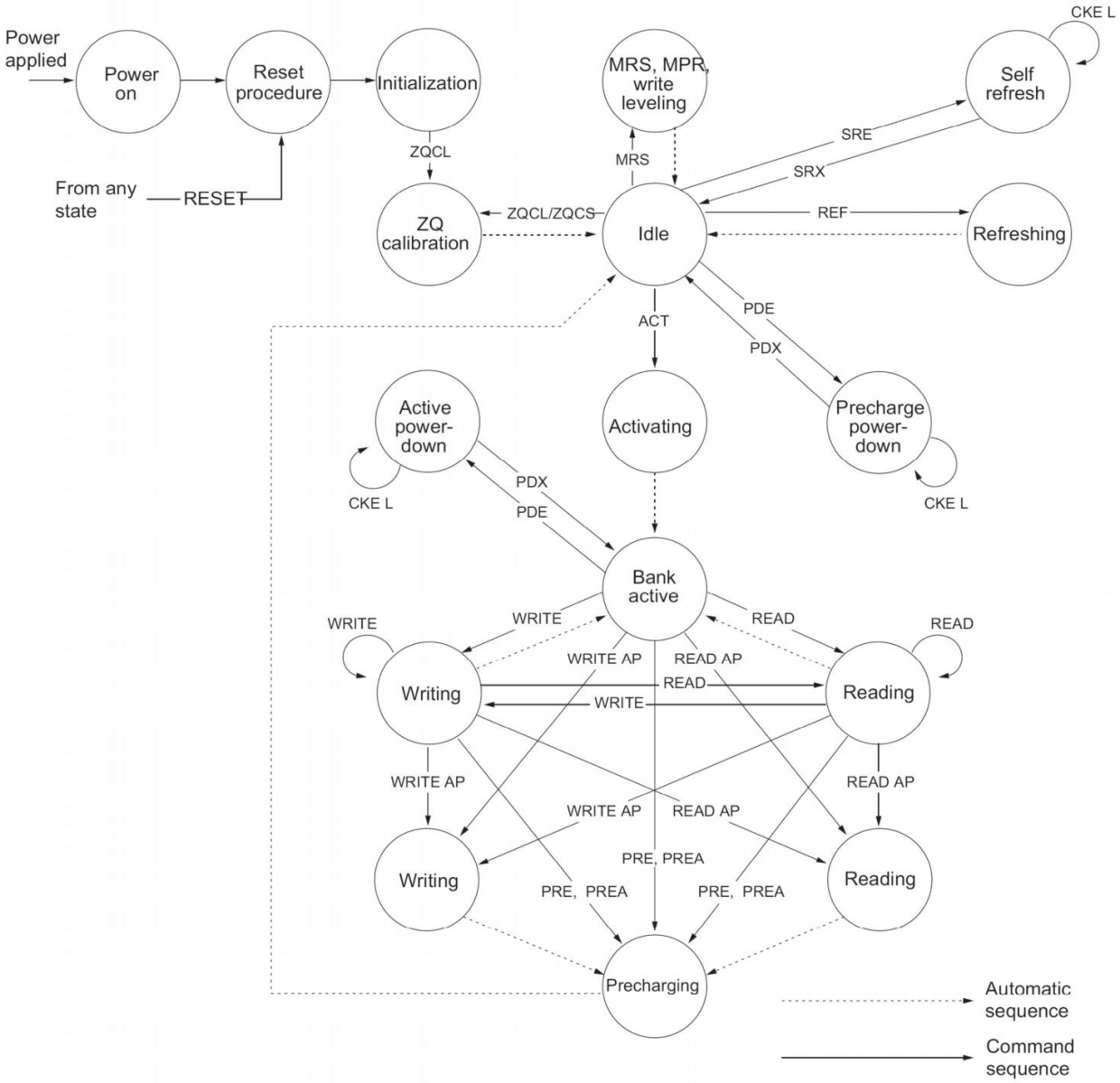
Note 4: Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

Note 5: Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

Note 6: Refer to DRAM supplier data sheet and/or SPD to determine if optional features or requirements are supported by DDR3/L SDRAM

Note 7: Read Burst type: Nibble Sequential, set MR0 A[3] =0B

Simplified State Diagram

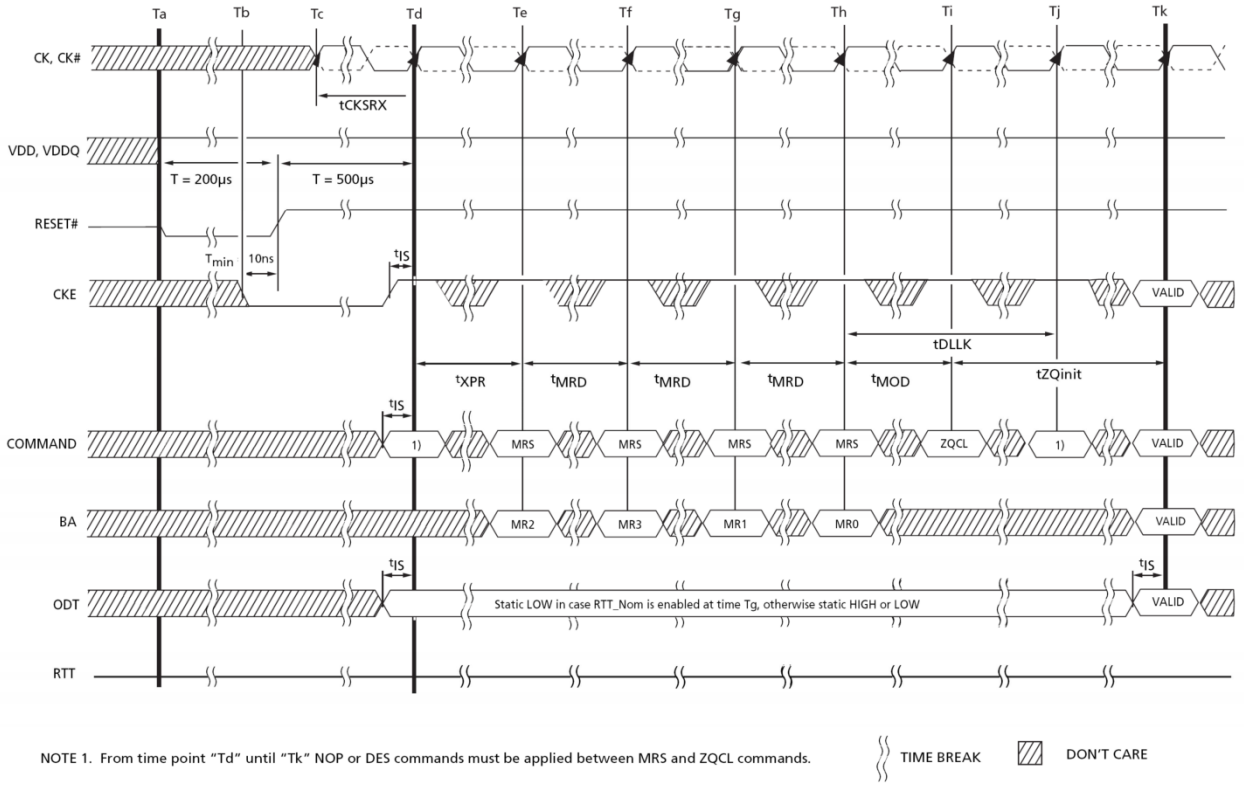


ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Reset and Power up Initialization Sequence



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Mode Register Setting

Mode Register 0 (MR0)

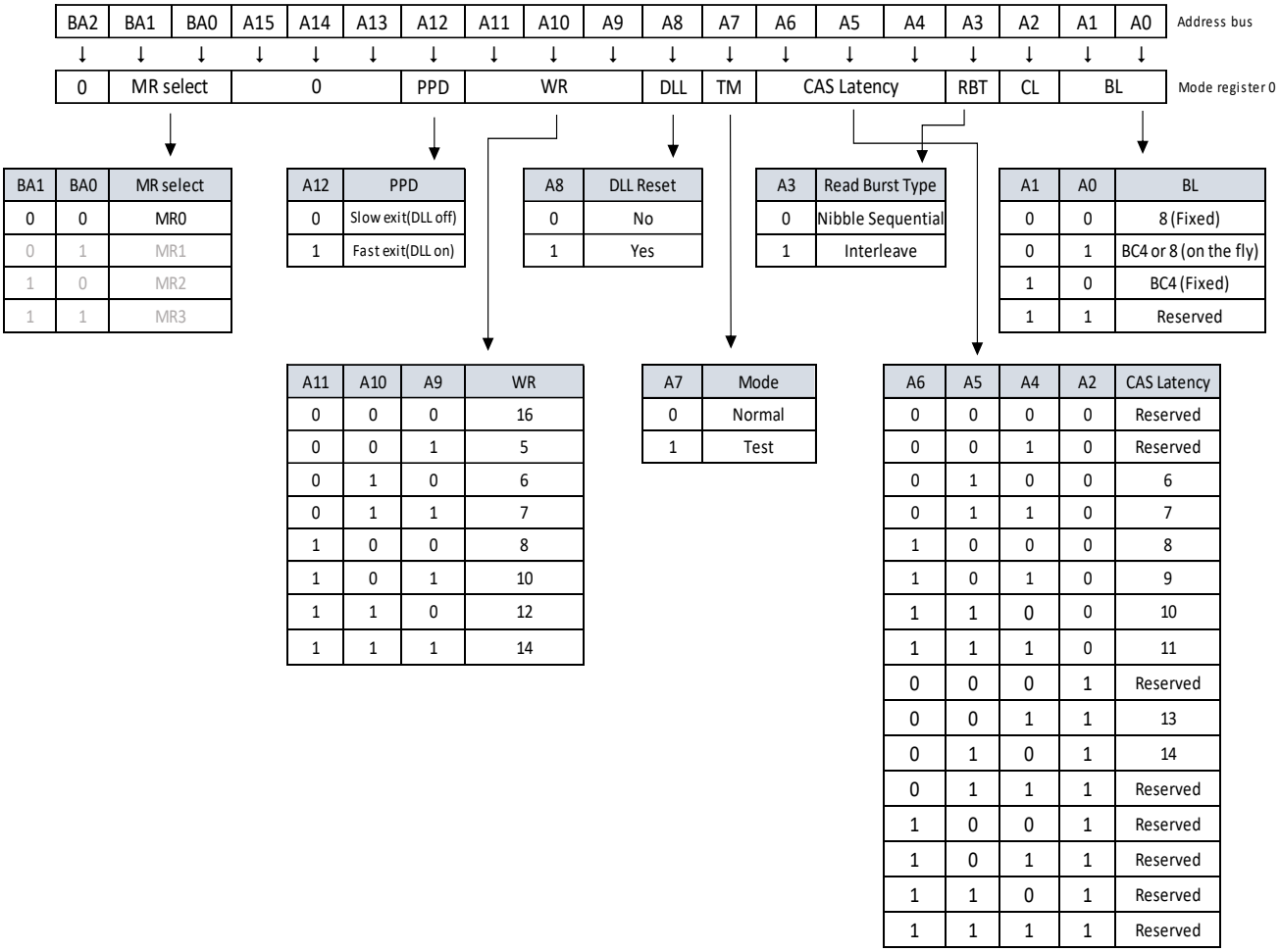
The base register, mode register 0 (MR0), is used to define various DDR3/L SDRAM modes of operation. These definitions include the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and pre-charge power-down mode.

Burst Length

Burst length is defined by MR0[1:0]. Read and write accesses to the DDR3/L SDRAM are burst-oriented, with the burst length being programmable to 4 (chop) mode, 8 (fixed) mode, or selectable using A12 during a READ/WRITE command (on-the-fly). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When MR0[1:0] is set to 01 during a READ/WRITE command, if A12 = 0, then BC4 mode is selected. If A12 = 1, then BL8 mode is selected. Specific timing diagrams, and turnaround between READ/WRITE, are shown in the READ/WRITE sections of this document.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[i:2] when the burst length is set to 4 and by A[i:3] when the burst length is set to 8, where Ai is the most significant column address bit for a given configuration. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Mode Register 0 (MR0) Definitions



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	PPD
0	Slow exit(DLL off)
1	Fast exit(DLL on)

A8	DLL Reset
0	No
1	Yes

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A11	A10	A9	WR
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

A7	Mode
0	Normal
1	Test

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	Reserved
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	Reserved
0	0	1	1	13
0	1	0	1	14
0	1	1	1	Reserved
1	0	0	1	Reserved
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

Note:
1. MR0[18, 15:13, 7] are reserved for future use and must be programmed to 0

Burst Type

Accesses within a given burst can be programmed to either a sequential or an interleaved order. The burst type is selected via MR0[3]. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address. DDR3/L only supports 4-bit burst chop and 8-bit burst access modes. Full interleave address ordering is supported for READs, while WRITEs are restricted to nibble (BC4) or word (BL8) boundaries.

Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
4(chop)	READ	0 0 0	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, Z, Z, Z, Z	1, 2
		0 0 1	1, 2, 3, 0, Z, Z, Z, Z	1, 0, 3, 2, Z, Z, Z, Z	1, 2
		0 1 0	2, 3, 0, 1, Z, Z, Z, Z	2, 3, 0, 1, Z, Z, Z, Z	1, 2
		0 1 1	3, 0, 1, 2, Z, Z, Z, Z	3, 2, 1, 0, Z, Z, Z, Z	1, 2
		1 0 0	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, Z, Z, Z, Z	1, 2
		1 0 1	5, 6, 7, 4, Z, Z, Z, Z	5, 4, 7, 6, Z, Z, Z, Z	1, 2
		1 1 0	6, 7, 4, 5, Z, Z, Z, Z	6, 7, 4, 5, Z, Z, Z, Z	1, 2
		1 1 1	7, 4, 5, 6, Z, Z, Z, Z	7, 4, 5, 6, Z, Z, Z, Z	1, 2
	WRITE	0 V V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 3, 4
		1 V V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	1, 3, 4,
8 (fixed)	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	1
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	1
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	1
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	1
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	1
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	1
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	1
	WRITE	V V V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1, 3

Notes:

1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
2. Z = Data and strobe output drivers are in tristate.
3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.
4. X = “Don’t Care.”

DLL Reset

DLL RESET is defined by MR0[8]. Programming MR0[8] to 1 activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of 0 after the DLL RESET function has been initiated.
Anytime the DLL RESET function is initiated, CKE must be HIGH and the clock held stable for 256 (tDLLK) clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization can result in invalid output timing specifications, such as tDQSCK timings.

Write Recovery

WRITE recovery time is defined by MR0[11:9]. Write recovery values of 5, 6, 7, 8, 10, or 12 can be used by programming MR0[11:9]. The user is required to program the correct value of write recovery, which is calculated by dividing tWR (ns) by tCK (ns) and rounding up a non-integer value to the next integer:
WR (cycles) = roundup (tWR (ns)/tCK (ns)).

Pre-charge Power-Down (Pre-charge PD)

The pre-charge power-down (pre-charge PD) bit applies only when pre-charge power-down mode is being used. When MR0[12] is set to 0, the DLL is off during pre-charge power-down, providing a lower standby current mode; however, tXPDLL must be satisfied when exiting. When MR0[12] is set to 1, the DLL continues to run during pre-charge power-down mode to enable a faster exit of pre-charge power-down mode; however, tXP must be satisfied when exiting.

CAS Latency (CL)

CAS latency (CL) is defined by MR0[6:4]. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. CL can be set to 5 through 14. DDR3/L SDRAM do not support half-clock latencies.

If an internal READ command is registered at clock edge n, and the CAS latency is m clocks, the data will be available nominally coincident with clock edge n + m. See Speed Bin Tables for the CLs supported at various operating frequencies.

Mode Register 1 (MR1)

The mode register 1 (MR1) controls additional functions and features not available in the other mode registers: Q OFF (OUTPUT DISABLE), TDQS (for the x8 configuration only), DLL ENABLE/DLL DISABLE, RTT,nom value (ODT), WRITE LEVELING, POSTED.

CAS ADDITIVE latency, and OUTPUT DRIVE STRENGTH. These functions are controlled via the bits. The MR1 register is programmed via the MRS command and retains the stored information until it is reprogrammed, until /RESET goes LOW, or until the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided it is performed correctly.

The MR1 register must be loaded when all banks are idle and no bursts are in progress. The controller must satisfy the specified timing parameters tMRD and tMOD before initiating a subsequent operation.

Mode Register 1 (MR1) Definition

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	Address bus
0	MR select		0			Qoff	TDQS	0	Rtt_Nom	0	Level	Rtt_Nom	D.I.C	AL		Rtt_Nom	D.I.C	DLL	Mode register 1

BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	Qoff
0	Output buffer enabled
1	Output buffer disabled

A11	TDQS
0	Disabled
1	Enabled

A4	A3	AL
0	0	Disabled
0	1	CL-1
1	0	CL-2
1	1	Reserved

A0	DLL Enable
0	Enabled
1	Disabled

A9	A6	A2	Rtt_Nom
0	0	0	Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12
1	0	1	RZQ/8
1	1	0	Reserved
1	1	1	Reserved

A7	Write Leveling enable
0	Disabled
1	Enabled

A5	A4	Output Driver Impedance
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

Notes:

1. MR1[18, 15:13, 10, 8] are reserved for future use and must be programmed to 0.
2. During write leveling, if MR1[7] and MR1[12] are 1, then all RTT,nom values are available for use.
3. During write leveling, if MR1[7] is a 1, but MR1[12] is a 0, then only RTT,nom write values are available for use.

DLL Enable/ DLL Disable

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering self refresh mode, the DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation. If the DLL is disabled prior to entering self refresh mode, the DLL remains disabled even upon exit of SELF REFRESH operation until it is re-enabled and reset.

The DRAM is not tested to check normal mode timings or functionality when the DLL is disabled. An attempt has been made to have the DRAM operate in the normal mode where reasonably possible when the DLL has been disabled; however, by industry standard, a few known exceptions are defined:

- ODT is not allowed to be used
- The output data is no longer edge-aligned to the clock
- CL and CWL can only be six clocks

When the DLL is disabled, timing and functionality can vary from the normal operation specifications when the DLL is enabled. Disabling the DLL also implies the need to change the clock frequency.

Output Drive Strength

The DDR3/L SDRAM uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5, 1]. RZQ/7 (34Ω [NOM]) is the primary output driver impedance setting for DDR3/L SDRAM devices. To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and VSSQ. The value of the resistor must be 240Ω ±1%.

The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation, and all data sheet timings and current specifications are met during an update. To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up, the DDR3/L SDRAM needs a calibration command that is part of the initialization and reset procedure.

Output Enable/ Disable

The OUTPUT ENABLE function is defined by MR1[12]. When enabled (MR1[12] = 0), all outputs (DQ, DQS, /DQS) function when in the normal mode of operation. When disabled (MR1[12] = 1), all DDR3/L SDRAM outputs (DQ and DQS, /DQS) are tri-stated. The output disable feature is intended to be used during IDD characterization of the READ current and during tDQSS margining (write leveling) only.

TDQS Enable

Termination data strobe (TDQS) is a feature of the x8 DDR3/L SDRAM configuration that provides termination resistance (RTT) and may be useful in some system configurations. TDQS is not supported in x4 or x16 configurations. When enabled via the mode register (MR1[11]), the RTT that is applied to DQS and /DQS is also applied to TDQS and /TDQS. In contrast to the RDQS function of DDR2 SDRAM, DDR3/L's TDQS provides the termination resistance RTT only. The OUTPUT DATA STROBE function of RDQS is not provided by TDQS; thus, RON does not apply to TDQS and /TDQS. The TDQS and DM functions share the same ball. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided, and the /TDQS ball is not used. The TDQS function is available in the x8 DDR3/L SDRAM configuration only and must be disabled via the mode register for the x4 and x16 configurations.

On-Die Termination

ODT resistance RTT,nom is defined by MR1[9, 6, 2]. The RTT termination value applies to the DQ, DM, DQS, /DQS, and TDQS, /TDQS balls. DDR3/L supports multiple RTT termination values based on RZQ/n where n can be 2, 4, 6, 8, or 12 and RZQ is 240Ω.

Unlike DDR2, DDR3/L ODT must be turned off prior to reading data out and must remain off during a READ burst. RTT,nom termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access, or when it is not in self refresh mode. Additionally, write accesses with dynamic ODT (RTT(WR)) enabled temporarily replaces RTT,nom with RTT(WR).

The actual effective termination, RTT(EFF), may be different from the RTT targeted due to nonlinearity of the termination. For RTT(EFF) values and calculations (see On-Die Termination (ODT). The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3/L SDRAM controller to independently turn on/off ODT for any or all devices. The ODT input control pin is used to determine when RTT is turned on (ODTL on) and off (ODTL off), assuming ODT has been enabled via MR1[9, 6, 2].Timings for ODT are detailed in On-Die Termination (ODT).

Write Leveling

The WRITE LEVELING function is enabled by MR1[7]. Write leveling is used (during initialization) to deskew the DQS strobe to clock offset as a result of fly-by topology designs. For better signal integrity, The EM47EM1688MBD/SBD adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology benefits from a reduced number of stubs and their lengths. However, fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM DQ byte on the EM47EM1688MBD/SBD. Controllers will have a difficult time maintaining t_{DQSS}, t_{DSS}, and t_{DSH} specifications without supporting write leveling in systems which use fly-by topology.

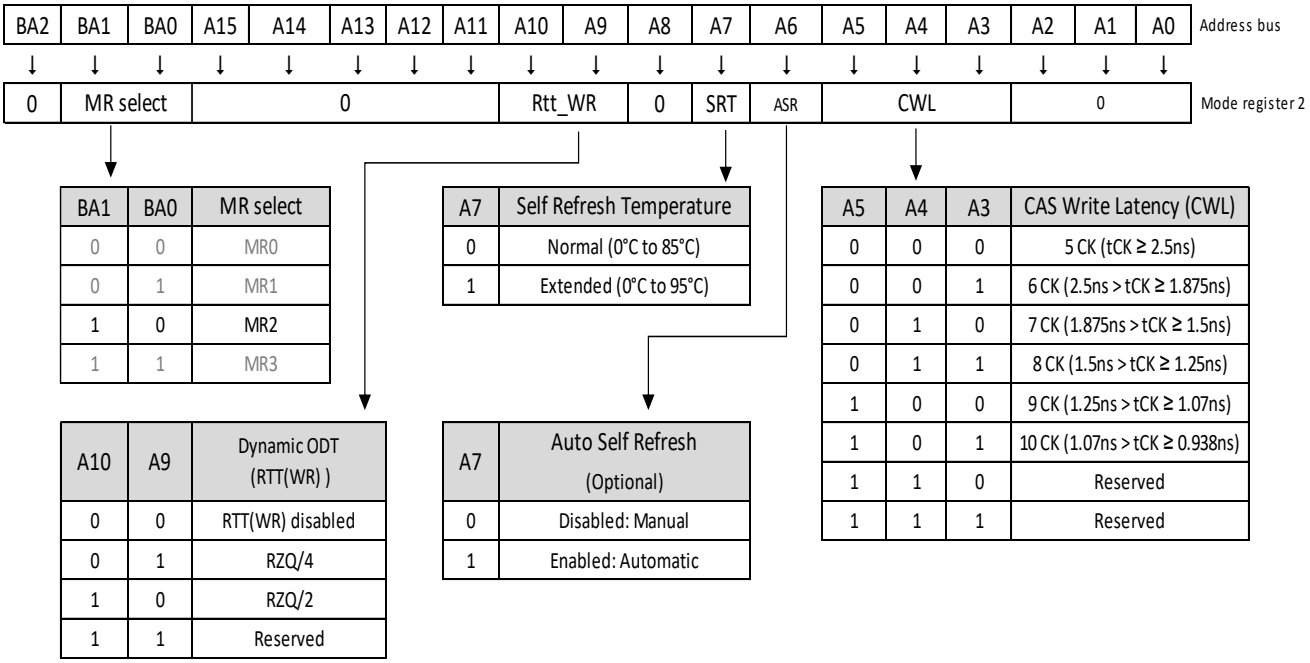
Posted CAS Additive Latency

POSTED CAS ADDITIVE latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR3/L SDRAM. MR1[4, 3] define the value of AL. MR1[4, 3] enable the user to program the DDR3/L SDRAM with AL = 0, CL - 1, or CL - 2.

Mode Register 2 (MR2)

The mode register 2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT), and DYNAMIC ODT (RTT(WR)). The MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is performed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time t_{MRD} and t_{MOD} before initiating a subsequent operation.

Mode Register 2 (MR2) Definition



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A7	Self Refresh Temperature
0	Normal (0°C to 85°C)
1	Extended (0°C to 95°C)

A5	A4	A3	CAS Write Latency (CWL)
0	0	0	5 CK (tCK ≥ 2.5ns)
0	0	1	6 CK (2.5ns > tCK ≥ 1.875ns)
0	1	0	7 CK (1.875ns > tCK ≥ 1.5ns)
0	1	1	8 CK (1.5ns > tCK ≥ 1.25ns)
1	0	0	9 CK (1.25ns > tCK ≥ 1.07ns)
1	0	1	10 CK (1.07ns > tCK ≥ 0.938ns)
1	1	0	Reserved
1	1	1	Reserved

A10	A9	Dynamic ODT (RTT(WR))
0	0	RTT(WR) disabled
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A7	Auto Self Refresh (Optional)
0	Disabled: Manual
1	Enabled: Automatic

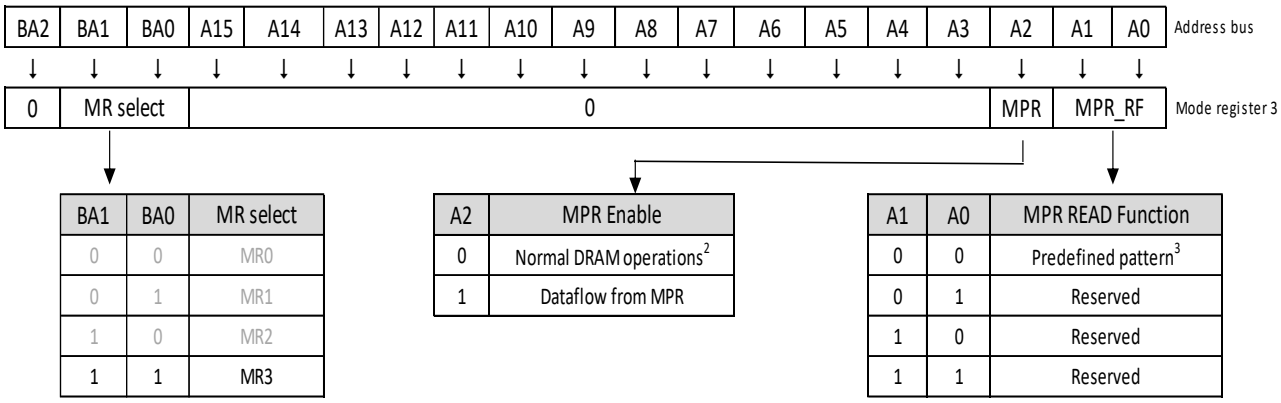
Note:

1. MR2[18, 15:11, 8, and 2:0] are reserved for future use and must all be programmed to 0.

Mode Register 3 (MR3)

The mode register 3 (MR3) controls additional functions and features not available in the other mode registers. Currently defined is the MULTIPURPOSE REGISTER (MPR). This function is controlled via the bits. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed again or until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided it is performed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time t_{MRD} and t_{MOD} before initiating a subsequent operation.

Mode Register 3 (MR3) Definition



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	MPR Enable
0	Normal DRAM operations[2]
1	Dataflow from MPR

A1	A0	MPR READ Function
0	0	Predefined pattern[3]
0	1	Reserved
1	0	Reserved
1	1	Reserved

Notes :

1. MR3[18 and 15:3] are reserved for future use and must all be programmed to 0.
2. When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
3. Intended to be used for READ synchronization.

Multi Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks pre-charged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-down mode, self-refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

DDR3/L-1600MHz Speed Bins

Speed Bin		DDR3/L-1600			
CL-t_{RCD}-t_{RP}		11-11-11			
Parameter		Symbol	Min	Max	Unit
Internal read command to first data		^tAA	13.75	-	ns
ACT to internal read or write delay time		^tRCD	13.75	-	ns
PRE command period		^tRP	13.75	-	ns
ACT to ACT or REF command period		^tRC	48.75	-	ns
ACT to PRE command period		^tRAS	35	9 x ^tREFI	ns
CL=5	CWL=5	$^tCK(AVG)$	3.0	3.3	ns
	CWL=6, 7, 8	$^tCK(AVG)$	Reserved	Reserved	ns
CL=6	CWL=5	$^tCK(AVG)$	2.5	3.3	ns
	CWL=6	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=7, 8	$^tCK(AVG)$	Reserved	Reserved	ns
CL=7	CWL=5	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=6	$^tCK(AVG)$	1.875	<2.5	ns
	CWL=7	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=8	$^tCK(AVG)$	Reserved	Reserved	ns
CL=8	CWL=5	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=6	$^tCK(AVG)$	1.875	<2.5	ns
	CWL=7	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=8	$^tCK(AVG)$	Reserved	Reserved	ns
CL=9	CWL=5, 6	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=7	$^tCK(AVG)$	1.5	<1.875	ns
	CWL=8	$^tCK(AVG)$	Reserved	Reserved	ns
CL=10	CWL=5, 6	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=7	$^tCK(AVG)$	1.5	<1.875	ns
	CWL=8	$^tCK(AVG)$	Reserved	Reserved	ns
CL=11	CWL=5, 6, 7	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=8	$^tCK(AVG)$	1.25	<1.5	ns
Supported CL Settings			5,6,7,8, 9,10,11		nCK
Supported CWL Settings			5,6,7,8		nCK

DDR3/L-1866MHz Speed Bins

Speed Bin		DDR3/L-1866			
CL-t_{RCD}-t_{RP}		13-13-13			
Parameter		Symbol	Min	Max	Unit
Internal read command to first data		^tAA	13.91	20	ns
ACT to internal read or write delay time		^tRCD	13.91	-	ns
PRE command period		^tRP	13.91	-	ns
ACT to ACT or REF command period		^tRC	47.91	-	ns
ACT to PRE command period		^tRAS	34	9 x ^tREFI	ns
CL=5	CWL=5	$^tCK(AVG)$	3.0	3.3	ns
	CWL=6, 7, 8	$^tCK(AVG)$	Reserved	Reserved	ns
CL=6	CWL=5	$^tCK(AVG)$	2.5	3.3	ns
	CWL=6, 7, 8, 9	$^tCK(AVG)$	Reserved	Reserved	ns
CL=7	CWL=5, 7, 8, 9	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=6	$^tCK(AVG)$	1.875	<2.5	ns
CL=8	CWL=5, 8, 9	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=6	$^tCK(AVG)$	1.875	<2.5	ns
	CWL=7	$^tCK(AVG)$	Reserved	Reserved	ns
CL=9	CWL=5, 6, 8, 9	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=7	$^tCK(AVG)$	1.5	<1.875	ns
CL=10	CWL=5, 6, 9	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=7	$^tCK(AVG)$	1.5	<1.875	ns
	CWL=8	$^tCK(AVG)$	Reserved	Reserved	ns
CL=11	CWL=5, 6, 7	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=8	$^tCK(AVG)$	1.25	<1.5	ns
	CWL=9	$^tCK(AVG)$	Reserved	Reserved	ns
CL=12	CWL=5, 6, 7, 8	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=9	$^tCK(AVG)$	Reserved	Reserved	ns
CL=13	CWL=5, 6, 7, 8	$^tCK(AVG)$	Reserved	Reserved	ns
	CWL=9	$^tCK(AVG)$	1.07	<1.25	ns
Supported CL Settings			5,6,7,8, 9,10,11,13		nCK
Supported CWL Settings			5,6,7,8,9		nCK

Electrical Characteristics and AC Operating Conditions -1

Parameter		Symbol	DDR3/L-1866		DDR3/L-1600		Unit	Notes
			Min	Max	Min	Max		
Clock Timing								
Clock period average: DLL disable mode	T_C = -55°C to 85°C	^tCK (DLL_DIS)	8	7800	8	7800	ns	9, 42
	T_C = >85°C to 95°C		8	3900	8	3900	ns	42
	T_C = >95°C to 105°C		8	3900	8	3900	ns	42
	T_C = >105°C to 125°C		8	3900	8	3900	ns	42
Clock period average: DLL enable mode		^tCK (AVG)	See Speed Bin Tables for ^tCK range allowed				ns	10, 11
High pulse width average		^tCH (AVG)	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		^tCL (AVG)	0.47	0.53	0.47	0.53	CK	12
Clock period jitter	DLL locked	^tJITper	–60	60	–70	70	ps	13
	DLL locking	$^tJITper,lck$	–50	50	–60	60	ps	13
Clock absolute period		^tCK (ABS)	MIN = ^tCK (AVG) MIN + ^tJITper MIN; MAX = ^tCK (AVG) MAX + ^tJITper MAX				ps	
Clock absolute high pulse width		^tCH (ABS)	0.43	–	0.43	–	^tCK (AVG)	14
Clock absolute low pulse width		^tCL (ABS)	0.43	–	0.43	–	^tCK (AVG)	15
Cycle-to-cycle jitter	DLL locked	^tJITcc	120		140		ps	16
	DLL locking	$^tJITcc,lck$	100		120		ps	16

Electrical characteristics and AC timing specification -2

Parameter		Symbol	DDR3/L-1866		DDR3/L-1600		Unit	Notes
			Min	Max	Min	Max		
Cumulative error across	2 cycles	^{t}ERR2per	–88	88	–103	103	ps	17
	3 cycles	^{t}ERR3per	–105	105	–122	122	ps	17
	4 cycles	^{t}ERR4per	–117	117	–136	136	ps	17
	5 cycles	^{t}ERR5per	–126	126	–147	147	ps	17
	6 cycles	^{t}ERR6per	–133	133	–155	155	ps	17
	7 cycles	^{t}ERR7per	–139	139	–163	163	ps	17
	8 cycles	^{t}ERR8per	–145	145	–169	169	ps	17
	9 cycles	^{t}ERR9per	–150	150	–175	175	ps	17
	10 cycles	^{t}ERR10per	–154	154	–180	180	ps	17
	11 cycles	^{t}ERR11per	–158	158	–184	184	ps	17
	12 cycles	^{t}ERR12per	–161	161	–188	188	ps	17
	n = 13, 14 . . . 49, 50cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*])×^{t}JITper MIN ^{t}ERR*n*per MAX = (1 + 0.68ln[*n*])×^{t}JITper MAX				ps	17
DQ Input Timing								
Data setup time to DQS, /DQS	Base (specification)@ 2 V/ns	^{t}DS (AC130)	70	–			ps	18, 19
	V_{REF} @ 2 V/ns		135	–			ps	19, 20
Data setup time to DQS, /DQS	Base (specification)@ 2 V/ns	^{t}DS (AC135)			25	–		
	V_{REF} @ 1 V/ns				160	–		
Data hold time from DQS, /DQS	Base (specification)@ 2 V/ns	^{t}DH (DC90)	75	–				
	@ 2 V/ns		110	–				
Data hold time from DQS, /DQS	Base (specification)@ 1V/ns	^{t}DH (DC90)			55	–	ps	18, 19
	V_{REF} @ 1 V/ns				145	–	ps	19, 20
Minimum data pulse width		^{t}DIPW	320	–	360	–	ps	41
DQ Output Timing								
DQS, /DQS to DQ skew, per access		^{t}DQSQ	–	85	–	100	ps	
DQ output hold time from DQS, /DQS		^{t}QH	0.38	–	0.38	–	^{t}CK (AVG)	21
DQ Low-Z time from CK, /CK		^{t}LZDQ	–390	195	–450	225	ps	22, 23
DQ High-Z time from CK, /CK		^{t}HZDQ	–	195	–	225	ps	22, 23
DQ Strobe Input Timing								
DQS, /DQS rising to CK, /CK rising		^{t}DQSS	–0.27	0.27	–0.27	0.27	CK	25
DQS, /DQS differential input low pulse width		^{t}DQSL	0.45	0.55	0.45	0.55	CK	

Electrical characteristics and AC timing specification -3

Parameter		symbol	DDR3/L-1866		DDR3/L-1600		Unit	Notes
			Min	Max	Min	Max		
DQS, /DQS differential input high pulse width		tDQSH	0.45	0.55	0.45	0.55	CK	
DQS, /DQS falling setup to CK, /CK rising		tDSS	0.18	–	0.18	–	CK	25
DQS, /DQS falling hold from CK, /CK rising		tDSH	0.18	–	0.18	–	CK	25
DQS, /DQS differential WRITE preamble		tWPRE	0.9	–	0.9	–	CK	
DQS, /DQS differential WRITE postamble		tWPST	0.3	–	0.3	–	CK	
DQ Strobe Output Timing								
DQS, /DQS rising to/from rising CK, /CK		tDQSCK	–195	195	–225	225	ps	23
DQS, /DQS rising to/from rising CK, /CK when DLL is disabled		tDQSCK (DLL_DIS)	1	10	1	10	ns	26
DQS, /DQS differential output high time		tQSH	0.40	–	0.40	–	CK	21
DQS, /DQS differential output low time		tQSL	0.40	–	0.40	–	CK	21
DQS, /DQS Low-Z time (RL - 1)		tLZDQS	–390	195	–450	225	ps	22, 23
DQS, /DQS High-Z time (RL + BL/2)		tHZDQS	–	195	–	225	ps	22, 23
DQS, /DQS differential READ preamble		tRPRE	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, /DQS differential READ postamble		tRPST	0.3	Note 27	0.3	Note 27	CK	23, 27
Command and Address Timing								
DLL locking time		tDLLK	512	–	512	–	CK	28
CTRL, CMD, ADDR setuptoCK,/CK	Base (specification)	tIS (AC160)			60	–	ps	29, 30,44
	V_{REF} @ 1 V/ns				220	–	ps	20, 30
CTRL, CMD, ADDR setuptoCK, /CK	Base (specification)	tIS (AC135)	65	–	185	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		200	–	320	–	ps	20, 30
CTRL, CMD, ADDR setuptoCK, /CK	Base (specification)	tIS (AC125)	150	–		–	ps	29, 30,44
	V_{REF} @ 1 V/ns		275	–		–	ps	20, 30
CTRL, CMD, ADDR hold from CK, /CK	Base (specification)	tIH (DC90)	110	–	130	–	ps	29, 30
	V_{REF} @ 1 V/ns		200	–	220	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		tIPW	535	–	560	–	ps	41
ACTIVATE to internal READ or WRITE delay		tRCD	See Speed Bin Tables for tRCD				ns	31
PRE-CHARGE command period		tRP	See Speed Bin Tables for tRP				ns	31
ACTIVATE-to-PRE-CHARGE command period		tRAS	See Speed Bin Tables for tRAS				ns	31, 32
ACTIVATE-to-ACTIVATE command period		tRC	See Speed Bin Tables for tRC				ns	31, 43

Electrical characteristics and AC timing specification -4

Parameter		Symbol	DDR3/L-1866		DDR3/L-1600		Unit	Notes
			Min	Max	Min	Max		
ACTIVATE-to-ACTIVATE Minimum command period	x4/x8/x16 (2KB page size)	tRRD	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 7.5ns		CK	31
Four ACTIVATE windows	x4/x8/x16 (2KB page size)	tFAW	35	–	40	–	ns	31
Write recovery time		tWR	MIN = 15ns; MAX = N/A				ns	31, 32,33
Delay from start of internal WRITE transaction to internal READ command		tWTR	MIN = greater of 4CK or 7.5ns; MAX = N/A				CK	31, 34
READ-to-PRE-CHARGE time		tRTP	MIN = greater of 4CK or 7.5ns; MAX = N/A				CK	31, 32
/CAS-to-/CAS command delay		tCCD	MIN = 4CK; MAX = N/A				CK	
Auto pre-charge write recovery + pre-charge time		tDAL	MIN = WR + tRP/tCK (AVG); MAX = N/A				CK	
MODE REGISTER SET command cycle time		tMRD	MIN = 4CK; MAX = N/A				CK	
MODE REGISTER SET command update delay		tMOD	MIN = greater of 12CK or 15ns; MAX = N/A				CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		tMPRR	MIN = 1CK; MAX = N/A				CK	
Calibration Timing								
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	MAX = N/A MIN = MAX(512nCK, 640ns)				CK	
	Normal operation	tZQoper	MAX = N/A MIN = MAX(256nCK, 320ns)				CK	
ZQCS command: Short calibration time		tZQCS	MAX = N/A MIN = MAX(64nCK, 80ns)				CK	
Initialization and Reset Timing								
Exit reset from CKE HIGH to a valid command		tXPR	MIN = greater of 5CK or tRFC + 10ns; MAX = N/A				CK	
Begin power supply ramp to power supplies stable		tVDDPR	MIN = N/A; MAX = 200				ms	
/RESET LOW to power supplies stable		tRPS	MIN = 0; MAX = 200				ms	
/RESET LOW to I/O and R_{TT} High-Z		tIOZ	MIN = N/A; MAX = 20				ns	35

Electrical characteristics and AC timing specification -5

Parameter		Symbol	DDR3/L-1866		DDR3/L-1600		Unit	Notes
			Min	Max	Min	Max		
Refresh Timing								
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC	MIN = 260; MAX = 70,200				ns	
Maximum refresh period	$T_C \leq 85°C$	–	64 (1X)				ms	36
	$T_C > 85°C$		32 (2X)				ms	36
	$T_C > 105°C$		8 (8X)				ms	36
Maximum average periodic refresh	$T_C \leq 85°C$	^{t}REFI	7.8 (64ms/8192)				µs	36
	$T_C > 85°C$		3.9 (32ms/8192)				µs	36
	$T_C > 105°C$		0.977 (8ms/8192)				µs	36
Self Refresh Timing								
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A				CK	
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN); MAX = N/A				CK	28
Minimum CKE low pulse width for self re fresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + CK; MAX = N/A				CK	
Valid clocks after self refresh entry or power-down entry		^{t}CKSRE	MIN = greater of 5CK or 10ns; MAX = N/A				CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	MIN = greater of 5CK or 10ns; MAX = N/A				CK	
Power-Down Timing								
CKE MIN pulse width		^{t}CKE (MIN)	Greater of 3CK or 5ns				CK	
Command pass disable delay		^{t}CPDED	MIN = 2; MAX = N/A		MIN = 1; MAX = N/A		CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX=9 x ^{t}REFI				CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL - 1CK				CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time				CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^{t}ANPD + ^{t}XPDLL				CK	

Electrical characteristics and AC timing specification -6

Parameter		Symbol	DDR3/L-1866		DDR3/L-1600		Unit	Notes
			Min	Max	Min	Max		
Power-Down Entry Minimum Timing								
ACTIVATE command to power-down entry		^{t}ACTPDEN	MIN = 2		MIN = 1		CK	
PRE-CHARGE/PRE-CHARGE ALL command to power-down entry		^{t}PRPDEN	MIN = 2		MIN = 1		CK	
REFRESH command to power-down entry		^{t}REFPDEN	MIN = 2		MIN = 1		CK	37
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)				CK	
READ/READ with auto pre-charge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1				CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)				CK	
	BC4MRS	^{t}WRPDEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)				CK	
WRITE with auto pre-charge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAPDEN	MIN = WL + 4 + WR + 1				CK	
	BC4MRS	^{t}WRAPDEN	MIN = WL + 2 + WR + 1				CK	
Power-Down Exit Timing								
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 6ns; MAX = N/A				CK	
Pre-charge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = N/A				CK	28
ODT Timing								
R_{TT} synchronous turn-on delay		ODTL on	CWL + AL - 2CK				CK	38
R_{TT} synchronous turn-off delay		ODTL off	CWL + AL - 2CK				CK	40
R_{TT} turn-on from ODTL on reference		^{t}AON	–195	195	–225	225	ps	23, 38
R_{TT} turn-off from ODTL off reference		^{t}AOF	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	MIN = 2; MAX = 8.5				ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		^{t}AOFPD	MIN = 2; MAX = 8.5				ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A				CK	

Electrical characteristics and AC timing specification -7

Parameter	Symbol	DDR3/L-1866		DDR3/L-1600		Unit	Notes
		Min	Max	Min	Max		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = N/A				CK	
Dynamic ODT Timing							
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew	ODTLcnw	WL - 2CK				CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4	ODTLcwn4	4CK + ODTLoff				CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8	ODTLcwn8	6CK + ODTLoff				CK	
R_{TT} dynamic change skew	^{t}ADC	0.3	0.7	0.3	0.7	CK	39
Write Leveling Timing							
First DQS, /DQS rising edge	^{t}WLMRD	40	–	40	–	CK	
DQS, /DQS delay	^{t}WLDQSEN	25	–	25	–	CK	
Write leveling setup from rising CK, /CK crossing to rising DQS, /DQS crossing	^{t}WLS	140	–	165	–	ps	
Write leveling hold from rising DQS, /DQS crossing to rising CK, /CK crossing	^{t}WLH	140	–	165	–	ps	
Write leveling output delay	^{t}WLO	0	7.5	0	7.5	ns	
Write leveling output error	^{t}WLOE	0	2.0	0	2.0	ns	

Notes:

1. AC timing parameters are valid from specified T_C MIN to T_C MAX values.
2. All voltages are referenced to V_{SS}.
3. Output timings are only valid for RON34 output buffer selection.
4. The unit ^{t}CK (AVG)) represents the actual ^{t}CK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and IDD tests may use a VIL-to-VIH swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^{t}IS, ^{t}IH, ^{t}DS, and ^{t}DH use the AC/DC trip points and CK, /CK and DQS, /DQS use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs (DQs are at 2V/ns for DDR3/L-1866 and DDR3/L-2133) and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
6. All timings that use time-based values (ns, µs, ms) should use ^{t}CK (AVG) to determine the correct number of clocks. In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQSdiff refers to the DQS and /DQS differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and /CK differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is V_{DDQ}/2 for single-ended signals and the crossing point for differential signals.
9. When operating in DLL disable mode, the DRAM is not warranted in compliance with normal mode timings or functionality.
10. The clock's ^{t}CK (AVG) is the average clock over any 200 consecutive clocks and ^{t}CK (AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^{t}CK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN.

12. The clock's ^{t}CH (AVG) and ^{t}CL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (^{t}JITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. ^{t}CH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. ^{t}CL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error ^{t}ERRnper, where n is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over n number of clock cycles.
18. ^{t}DS (base) and ^{t}DH (base) values are for a single-ended 1 V/ns slew rate DQs (DQs are at 2 V/ns for DDR3/L-1866 and DDR3/L-2133) and 2 V/ns slew rate differential DQS, /DQS; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, /DQS) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to VREF when the slew rate is 1 V/ns (DQs are at 2V/ns for DDR3/L-1866 and DDR3/L-2133). These values, with a slew rate of 1 V/ns (DQs are at 2V/ns for DDR3/L-1866 and DDR3/L-2133), are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JITper (larger of ^{t}JITper (MIN) or ^{t}JITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting tERR10per (MAX): ^{t}DQSCK (MIN), ^{t}LZDQS (MIN), ^{t}LZDQ (MIN), and ^{t}AON (MIN). The following parameters are required to be derated by subtracting ^{t}ERR10per (MIN): ^{t}DQSCK (MAX), ^{t}HZ (MAX), ^{t}LZDQS (MAX), ^{t}LZDQ (MAX), and ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX) is derated by subtracting ^{t}JITper (MIN).
24. The maximum preamble is bound by ^{t}LZDQS (MAX).
25. These parameters are measured from a data strobe signal (DQS, /DQS) crossing to its respective clock signal (CK, /CK) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The ^{t}DQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by ^{t}HZDQS (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency tXPDLL, timing must be met.
29. ^{t}IS (base) and ^{t}IH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, /CK differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, /CK) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3/L SDRAM device supports ^{t}nPARAM (nCK) = RU(^{t}PARAM [ns]/^{t}CK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}nRP (nCK) = RU(^{t}RP/^{t}CK[AVG]) if all input clock jitter specifications are met. This means that for DDR3/L-800 6-6-6, of which tRP = 5ns, the device will support ^{t}nRP = RU(^{t}RP/^{t}CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRE-CHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto pre-charge, the DDR3/L SDRAM will hold off the internal PRE-CHARGE command until ^{t}RAS (MIN) has been satisfied.
33. When operating in DLL disable mode, the greater of 5CK or 15ns is satisfied for tWR.

34. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. /RESET should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until /RESET is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms when TC is less than or equal to 85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When TC is greater than 85°C, the refresh period is 32ms. When TC is greater than 105°C, the refresh period is 8ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when ^{t}REFPDEN (MIN) is satisfied, there are cases where additional time such as ^{t}XPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. This output load is used for ODT timings. Designs that were created prior to JEDEC tightening the maximum limit from 9ns to 8.5ns will be allowed to have a 9ns maximum.
39. Half-clock output parameters must be derated by the actual tERR10per and ^{t}JITdty when input clock jitter is present. This results in each parameter becoming larger. The parameters ^{t}ADC (MIN) and tAOF (MIN) are each required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX). The parameters ^{t}ADC (MAX) and ^{t}AOF (MAX) are required to be derated by subtracting both ^{t}ERR10per (MAX) and ^{t}JITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z.
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than ^{t}RFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRE-CHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other VIH(AC) value may be used for data inputs.

    For example, for DDR3/L-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3/L-800, the address/ command inputs must use either $V_{IH(AC175)}$,min with ^{t}IS(AC175) of 200ps or $V_{IH(AC150),min}$ with ^{t}IS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with ^{t}DS(AC175) of 75ps or $V_{IH(AC150),min}$ with ^{t}DS(AC150) of 125ps.

Package Description: 96Ball-FBGA (8x13 mm)