

Revision History

Revision 0.1 (Jul. 2010)

- First release.

Features

- Fully Synchronous to Positive Clock Edge
- JEDEC Standard 1.8V Power Supply
- LVCMOS Compatible with Multiplexed Address
- Programmable Burst Length (B/L) - 1, 2, 4, 8 or Full Page
- Programmable CAS Latency (C/L) - 2 or 3
- Data Mask (DQM) for Read / Write Masking
- Programmable Wrap Sequence
 - Sequential (B/L = 1/2/4/8/full Page)
 - Interleave (B/L = 1/2/4/8)
- Burst Read with Single-bit Write Operation
- All Inputs are sampled at the Rising Edge of the System Clock
- Support Deep Power Down Mode
- Partial Array Self Refresh (PASR)
- Auto Temperature Compensated Self Refresh (Auto TCSR)
- Driver Strength (DS)
- Auto Refresh and Self Refresh
- 4,096 Refresh Cycles / 64ms (15.625us)

Description

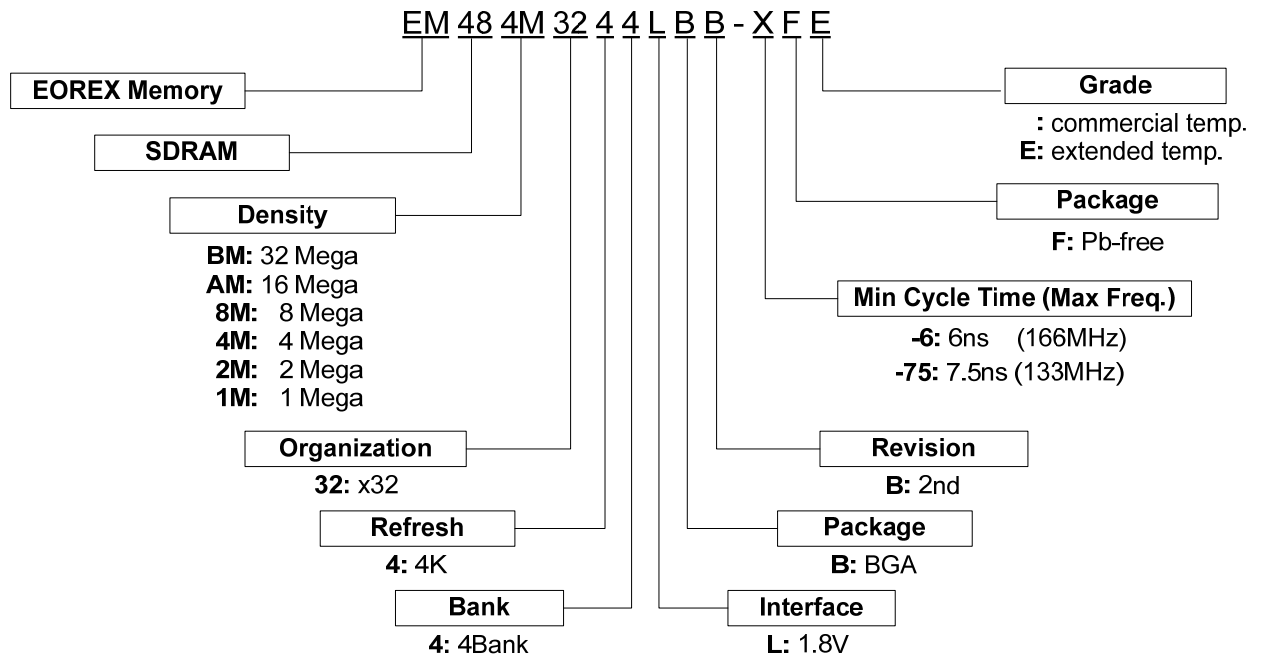
The EM484M3244LBB is Mobile Synchronous Dynamic Random Access Memory (Mobile SDRAM) organized as 1Meg words x 4 banks by 32 bits. All inputs and outputs are synchronized with the positive edge of the clock.

The 128Mb Mobile SDRAM uses synchronized pipelined architecture to achieve high speed data transfer rates and is designed to operate at 1.8V ultra low power memory system. It also provides auto refresh with deep power saving / down mode. The data paths are internally pipelined to achieve very high bandwidth. All inputs and outputs voltage levels are compatible with LVCMOS.

Available packages: TFBGA-90B (13mmx8mm).

Ordering Information

Part No	Organization	Max. Freq	Package	Grade	Pb
EM484M3244LBB-75F	4M X 32	133MHz @CL3	TFBGA -90B	Commercial	Free
EM484M3244LBB-6F	4M X 32	166MHz @CL3	TFBGA -90B	Commercial	Free
EM484M3244LBB-75FE	4M X 32	133MHz @CL3	TFBGA -90B	Extend	Free
EM484M3244LBB-6FE	4M X 32	166MHz @CL3	TFBGA -90B	Extend	Free



* EOREX reserves the right to change products or specification without notice.

Pin Assignment

1	2	3		7	8	9
DQ26	DQ24	VSS	A	VDD	DQ23	DQ21
DQ28	VDDQ	VSSQ	B	VDDQ	VSSQ	DQ19
VSSQ	DQ27	DQ25	C	DQ22	DQ20	VDDQ
VSSQ	DQ29	DQ30	D	DQ17	DQ18	VDDQ
VDDQ	DQ31	NC	E	NC	DQ16	VSSQ
VSS	DQM3	A3	F	A2	DQM2	VDD
A4	A5	A6	G	A10	A0	A1
A7	A8	NC	H	NC	BA1	A11
CLK	CKE	A9	J	BA0	/CS	/RAS
DQM1	NC	NC	K	/CAS	/WE	DQM0
VDDQ	DQ8	VSS	L	VDD	DQ7	VSSQ
VSSQ	DQ10	DQ9	M	DQ6	DQ5	VDDQ
VSSQ	DQ12	DQ14	N	DQ1	DQ3	VDDQ
DQ11	VDDQ	VSSQ	P	VDDQ	VSSQ	DQ4
DQ13	DQ15	VSS	R	VDD	DQ0	DQ2

90ball TFBGA / (13mm x 8mm)

Pin Description (Simplified)

Pin	Name	Function
J1	CLK	(System Clock) Master clock input (Active on the positive rising edge)
J8	/CS	(Chip Select) Selects chip when active
J2	CKE	(Clock Enable) Activates the CLK when "H" and deactivates when "L". CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
G8,G9,F7,F3,G1, G2,G3,H1,H2,J3, G7,H9	A0~A11	(Address) Row address (A0 to A11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. CA (CA0 to CA7) is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the pre-charge mode. When A10= High at the pre-charge command cycle, all banks are pre-charged. But when A10= Low at the pre-charge command cycle, only the bank that is selected by BA is pre-charged.
J7,H8	BA0,BA1	(Bank Address) Selects which bank is to be active.
J9	/RAS	(Row Address Strobe) Latches Row Addresses on the positive rising edge of the CLK with /RAS "L". Enables row access & pre-charge.
K7	/CAS	(Column Address Strobe) Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
K8	/WE	(Write Enable) Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
K9,K1,F8,F2	DQM0~DQM3	(Data Input/Output Mask) DQM controls I/O buffers.
R8,N7,R9,N8,P9, M8,M7,L8,L2,M3, M2,P1,N2,R1,N3, R2,E8,D7,D8,B9, C8,A9,C7,A8,A2, C3,A1,C2,B1,D2, D3,E2	DQ0~DQ31	(Data Input/Output) DQ pins have the same function as I/O pins on a conventional DRAM.
A7,F9,L7,R7/ A3,F1,L3,R3	V _{DD} /V _{SS}	(Power Supply/Ground) V _{DD} and V _{SS} are power supply pins for internal circuits.
B2,B7,C9,D9,E1, L1,M9,N9,P2/B8, B3,C1,D1,E9,L9, M1,N1,P8	V _{DDQ} /V _{SSQ}	(Power Supply/Ground) V _{DDQ} and V _{SSQ} are power supply pins for the output buffers.
E3,E7,H3,H7,K2, K3	NC	(No Connection) This pin is recommended to be left No Connection on the device.

Absolute Maximum Rating

Symbol	Item	Rating	Units
V _{IN} , V _{OUT}	Input, Output Voltage	-1.0 ~ +2.6	V
V _{DD} , V _{DDQ}	Power Supply Voltage	-1.0 ~ +2.6	V
T _{OP}	Operating Temperature Range	Commercial	0 ~ +70
		Extended	-25 ~ +85
T _{STG}	Storage Temperature Range	-55 ~ +150	°C
P _D	Power Dissipation	1	W
I _{OS}	Short Circuit Current	50	mA

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (V_{CC}=1.8V, f=1MHz, T_A=25°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
C _{CLK}	Clock Capacitance	2.0	-	4.0	pF
C _I	Input Capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML, DQMU	2.0	-	4.0	pF
C _O	Input/Output Capacitance	2.0	-	6.0	pF

Recommended DC Operating Conditions (T_A=-25°C ~85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{DD}	Power Supply Voltage	1.7	1.8	1.95	V
V _{DDQ}	Power Supply Voltage (for I/O Buffer)	1.7	1.8	1.95	V
V _{IH}	Input Logic High Voltage	0.8*V _{DDQ}	-	V _{DDQ} +0.3	V
V _{IL}	Input Logic Low Voltage	-0.3	0	0.3	V

Note: * All voltages referred to V_{SS}.

* V_{IH} (max.) = 2.2V for pulse width ≤ 3ns

* V_{IL} (min.) = -1.0V for pulse width ≤ 3ns

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _{IL}	Input Leakage Current	0 ≤ V _I ≤ V _{DDQ} , V _{DDQ} = V _{DD} All other pins not under test = 0V	-1	-	+1	uA
I _{OL}	Output Leakage Current	0 ≤ V _O ≤ V _{DDQ} , D _{OUT} is disabled	-1.5	-	+1.5	uA
V _{OH}	High Level Output Voltage	I _O = -1mA	V _{DDQ} -0.2	-	-	V
V _{OL}	Low Level Output Voltage	I _O = +1mA	-	-	0.2	V

Recommended DC Operating Conditions

($V_{DD}=1.7 \sim 1.95V$, $T_A=-25^{\circ}C \sim 85^{\circ}C$)

Symbol	Parameter	Test Conditions	Max.		Units	
			-6	-75		
I_{CC1}	Operating Current <i>(Note 1)</i>	Burst length=1, $t_{RC} \geq t_{RC}(\text{min.})$, $I_{OL}=0\text{mA}$, One bank active	60	50	mA	
I_{CC2P}	Precharge Standby Current in Power Down Mode	$\text{CKE} \leq V_{IL}(\text{max.})$, $t_{CK}=10\text{ns}$	0.1	0.1	mA	
I_{CC2PS}		$\text{CKE} \leq V_{IL}(\text{max.})$, $t_{CK} = \infty$	0.1	0.1	mA	
I_{CC2N}	Precharge Standby Current in Non-power Down Mode	$\text{CKE} \geq V_{IH}(\text{min.})$, $t_{CK}=10\text{ns}$, $/\text{CS} \geq V_{IH}(\text{min.})$ Input signals are changed one time during 2 clocks	10	10	mA	
I_{CC2NS}		$\text{CKE} \geq V_{IH}(\text{min.})$, $t_{CK} = \infty$, $\text{CLK} \leq V_{IL}(\text{max.})$ Input signals are stable	5	5	mA	
I_{CC3P}	Active Standby Current in Power Down Mode	$\text{CKE} \leq V_{IL}(\text{max.})$, $t_{CK}=10\text{ns}$	3	3	mA	
I_{CC3PS}		$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max.})$, $t_{CK} = \infty$	3	3	mA	
I_{CC3N}	Active Standby Current in Non-power Down Mode	$\text{CKE} \geq V_{IH}(\text{min.})$, $t_{CK}=10\text{ns}$, $/\text{CS} \geq V_{IH}(\text{min.})$ Input signals are changed one time during 2 clocks	20	20	mA	
I_{CC3NS}		$\text{CKE} \geq V_{IH}(\text{min.})$, $t_{CK} = \infty$, $\text{CLK} \leq V_{IL}(\text{max.})$ Input signals are stable	8	8	mA	
I_{CC4}	Operating Current (Burst Mode) <i>(Note 2)</i>	$t_{CCD}=1\text{CLKs}$, $I_{OL}=0\text{Ma}$ $t_{CK} > t_{CK}(\text{min.})$, Page Burst All banks activated	90	80	mA	
I_{CC5}	Refresh Current <i>(Note 3)</i>	$t_{RC} \geq t_{RFC}(\text{min.})$, all banks active	70	70	mA	
I_{CC6}	Self Refresh Current	$\text{CKE} \leq 0.2V$	Internal TCSR	Max 40	Max 85	$^{\circ}C$
			Full Array	120	200	μA
			1/2 Full Array	100	160	μA
			1/4 Full Array	90	140	μA
I_{CC7}	Deep Power Down Mode Current	-	10	10	μA	

*All voltages referenced to V_{SS} .

Note 1: I_{CC1} depends on output loading and cycle rates.

Specified values are obtained with the output open.

Input signals are changed only one time during t_{CK} (min.)

Note 2: I_{CC4} depends on output loading and cycle rates.

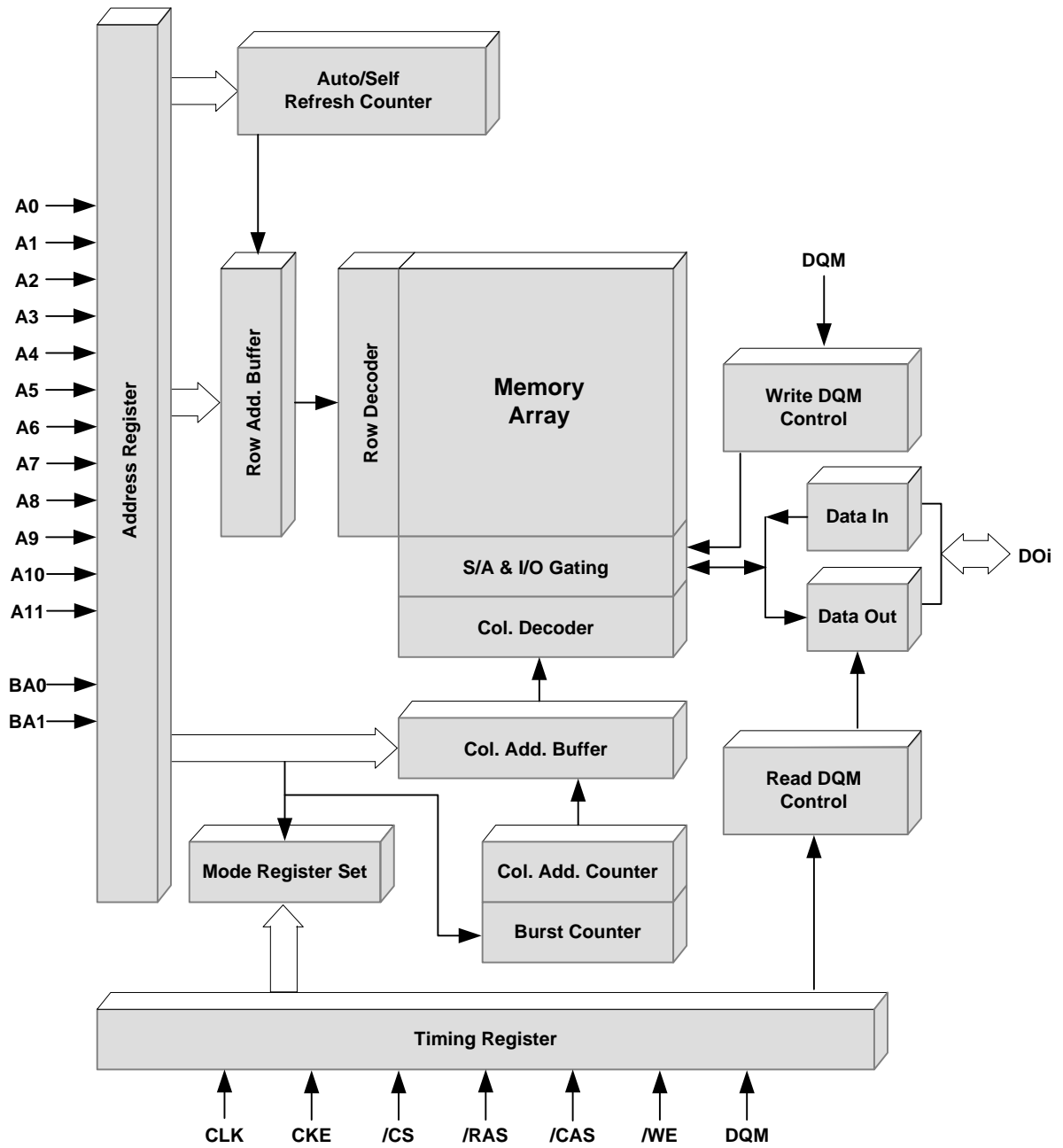
Specified values are obtained with the output open.

Input signals are changed only one time during t_{CK} (min.)

Note 3: Input signals are changed only one time during t_{CK} (min.)

Note 4: Standard power version.

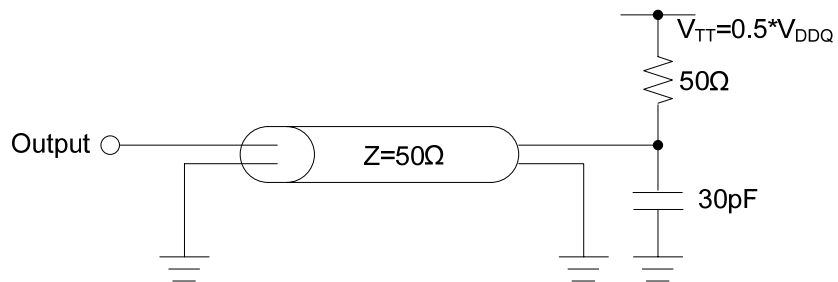
Block Diagram



AC Operating Test Conditions

($V_{DD}=1.7 \sim 1.95V$, $T_A=-25^{\circ}C \sim 85^{\circ}C$)

Item	Conditions
Output Reference Level	$0.5 * V_{DDQ}$
Output Load	See diagram as below
Input Signal Level	$0.9 * V_{DDQ} / 0.2V$
Transition Time of Input Signals	1/1 ns
Input Reference Level	$0.5 * V_{DDQ}$



AC Operating Test Characteristics

(AC operation conditions unless otherwise noted)

Symbol	Parameter	-6		-75		Units	
		Min.	Max.	Min.	Max.		
t _{CK}	Clock Cycle Time	CL=3	6	1000	7.5	1000	ns
		CL=2	10	1000	10	1000	
t _{AC}	Access Time form CLK	CL=3	-	5.4	-	6	ns
		CL=2	-	8	-	8	
t _{CH}	CLK High Level Width		2	-	2.5	-	ns
t _{CL}	CLK Low Level Width		2	-	2.5	-	ns
t _{CKS}	CLK Setup Time		1.5	-	1.5	-	ns
t _{CKH}	CLK Hold Time		1	-	1	-	ns
t _{OH}	Data-out Hold Time	CL=3	2.5	-	3	-	ns
		CL=2	2.5	-	3	-	
t _{HZ}	Data-out High Impedance Time <i>(Note 5)</i>	CL=3	-	5.4	-	6	ns
		CL=2	-	8	-	8	
t _{LZ}	Data-out Low Impedance Time		1	-	1	-	ns
t _{IH}	Input Hold Time		1	-	1	-	ns
t _{IS}	Input Setup Time		1.5	-	1.5	-	ns

* All voltages referenced to V_{SS}.**Note 5:** t_{HZ} defines the time at which the output achieve the open circuit condition and is not referenced to output voltage levels.

AC Operating Test Characteristics (Continued)

(AC operation conditions unless otherwise noted)

Symbol	Parameter	-6		-75		Units	
		Min.	Max.	Min.	Max.		
t_{RC}	ACTIVE to ACTIVE Command Period (Note 6)	60	-	67.5	-	ns	
t_{RAS}	ACTIVE to PRECHARGE Command Period (Note 6)	42	100K	45	100K	ns	
t_{RP}	PRECHARGE to ACTIVE Command Period (Note 6)	18	-	22.5	-	ns	
t_{RCD}	ACTIVE to READ/WRITE Delay Time (Note 6)	18	-	22.5	-	ns	
t_{RRD}	ACTIVE(one) to ACTIVE(another) Command (Note 6)	12	-	15	-	ns	
t_{CCD}	READ/WRITE Command to READ/WRITE Command	1	-	1	-	CLK	
t_{WR}	Date-in to PRECHARGE Command	12	-	15	-	CLK	
t_{BDL}	Last data-in to burst Stop command	1	-	1	-	CLK	
t_{ROH}	Data-out to High Impedance from PRECHARGE Command	CL=3	3	-	3	-	CLK
		CL=2	2	-	2	-	
t_{MRD}	Load MRS register command to Active or Refresh command	2	-	2	-	CLK	
t_{CDL}	Last data-in to new Read/Write command	1	-	1	-	CLK	
t_{RFC}	Auto Refresh Period	110	-	110	-	ns	
t_{XSR}	Exit Slef Refresh to Active command	110	-	110	-	ns	
t_{REF}	Refresh Time (4,096 cycle)	-	64	-	64	ms	

* All voltages referenced to V_{SS} .

Note 6: These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows:

The number of clock cycles = Specified value of timing/clock period (Count Fractions as a whole number)

Recommended Power On and Initialization

The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs. (Like a conventional DRAM) During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed $V_{DD}+0.3V$ on any of the input pins or V_{DD} supplies. (CLK signal started at same time)

After power on and applied VDD, VDDQ and the clock are stable; an initial pause of 200 μs is required followed by a precharge of all banks using the precharge command. (All banks in idle state)

To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required, and these may be done before or after programming the Mode Register.

Temperature Compensated Self Refresh

In order to save power consumption, Mobile SDRAM includes the internal temperature sensor and units to control the self refresh cycle automatically according to the two temperature range ; 40°C (max.), 85°C (max.).

Temperature Range	Self Refresh Current (I_{CC6})			
	Full Array	1/2 Array	1/4 Array	Unit
Max.40°C	120	100	90	μA
Max.85°C	200	160	140	μA

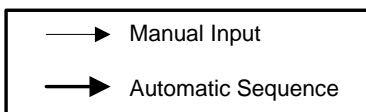
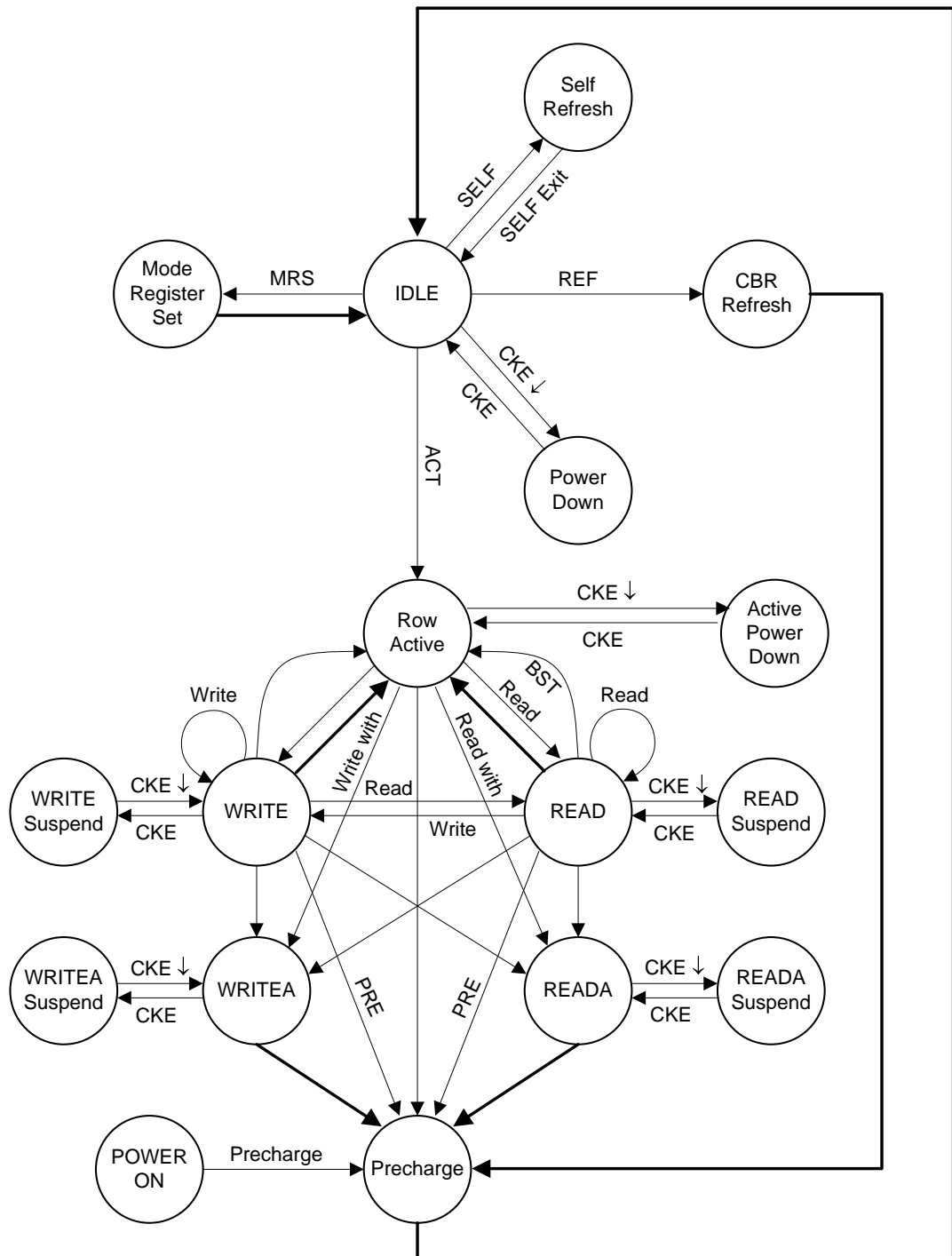
Partial Array Self Refresh

For further power savings during Self Refresh, the PASR feature allows selecting the amount of memory that will be refreshed during Self Refresh. The refresh options are all banks (banks 0, 1, 2 and 3); two banks (banks 0 and 1); and one bank (bank 0). Write and Read commands can still occur during standard operation, but only the selected banks will be refreshed during Self Refresh. Data in banks that are disabled will be lost.

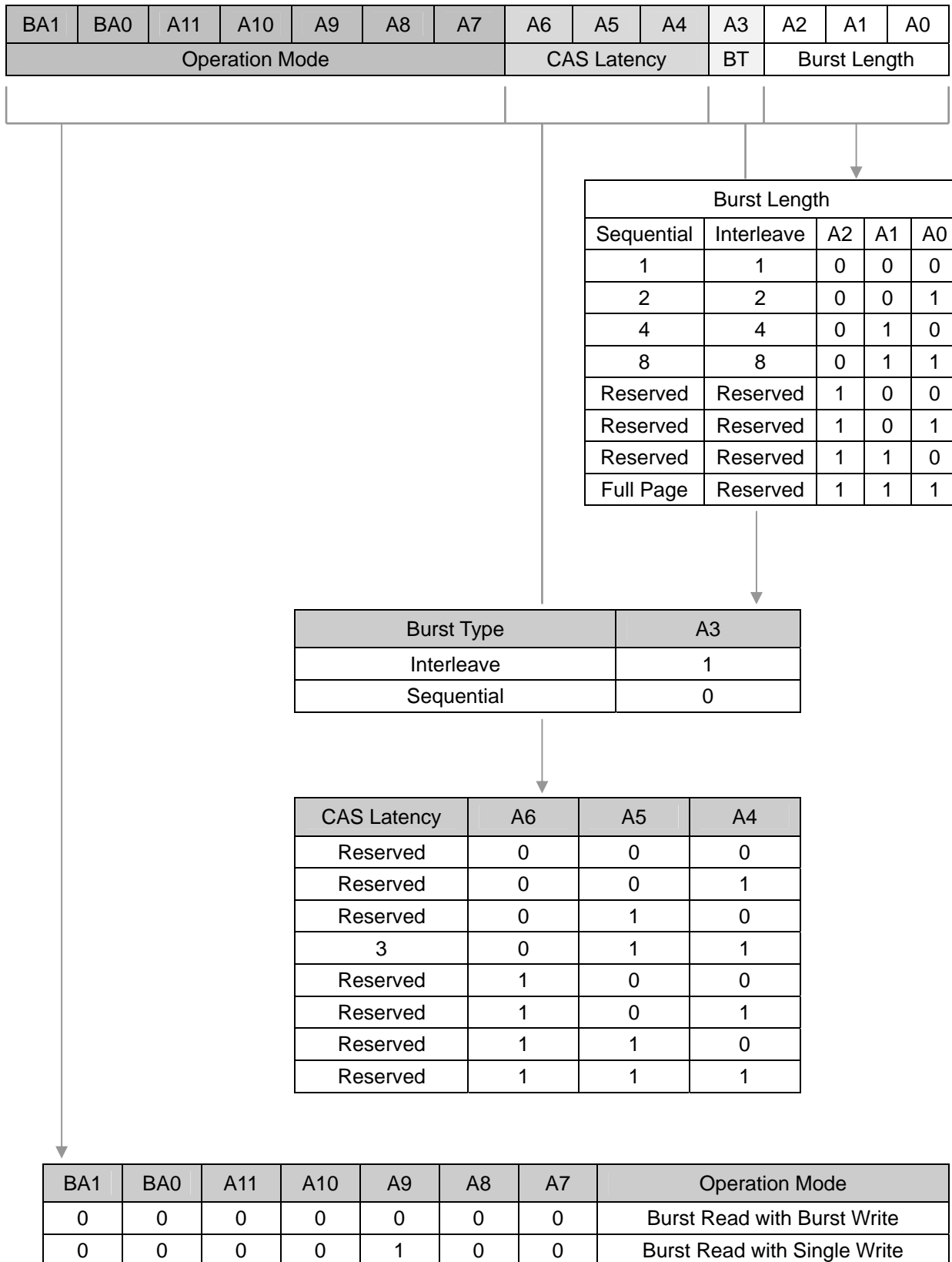
Deep Power Down

Deep power down is an operating mode to achieve maximum power reduction by eliminating the power of the whole memory array of the devices. Data will not be retained once the device enters deep power down mode. This mode is entered by having all banks idle then /CS and /WE held low with /RAS and /CAS held high at the rising edge of the clock, while CKE is low. To assert CKE high for exit deep power down mode.

Simplified State Diagram



Address Input for Mode Register Set (MRS)



Address Input for Extended Mode Register Set (EMRS)

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	DS		0	0	PASR		

↓

Partial Array Self Refresh			
Select	A2	A1	A0
All banks	0	0	0
1/2 banks (BA1=0)	0	0	1
1/4 banks (BA1=BA0=0)	0	1	0
Reserved	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

↓

Driver Strength	A6	A5
Full Strength	0	0
1/2 Full Strength	0	1
1/4 Full Strength	1	0
1/8 Full Strength	1	1

Note: BA1 must be set to "1" to select the Extended Mode Register Set.

Burst Type (A3)

Burst Length	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	0	0 1	0 1
	X	X	0	1 0	1 0
4	X	0	0	0 1 2 3	0 1 2 3
	X	0	1	1 2 3 0	1 0 3 2
	X	1	0	2 3 0 1	2 3 0 1
	X	1	1	3 0 1 2	3 2 1 0
8	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0	
Full Page*	n	n	n	Cn Cn+1 Cn+2.....	-

* Page length is a function of I/O organization and column addressing $\times 32$ (CA0 ~ CA7):

Full page = 256bits

1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A11, A9~A10
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	BSTH	H	H	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	X	L	H	L	L	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Precharge Select Bank	PRE	H	X	L	L	H	L	V	L	X
Precharge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V
Extended Mode Register Set	EMRS	H	X	L	L	L	L	L	L	V
Auto Refresh	-	H	H	L	L	L	H	X	X	X
Self Refresh Entry	-	H	L	L	L	L	H	X	X	X
Self Refresh Exit	-	L	H	H	X	X	X	X	X	X
				L	H	H	H	X	X	X
Precharge Power Down Entry	-	H	L	H	X	X	X	X	X	X
				L	H	H	H	X	X	X
Precharge Power Down Exit	-	L	H	H	X	X	X	X	X	X
				L	H	H	H	X	X	X
Clock Suspend Entry	-	H	L	H	X	X	X	X	X	X
				L	V	V	V	X	X	X
Clock Suspend Exit	-	L	H	X	X	X	X	X	X	X
Deep Power Down Entry	-	H	L	L	H	H	L	X	X	X
Deep Power Down Exit	-	L	H	X	X	X	X	X	X	X

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. Operative Command Table (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	NOP or power down <small>(Note 8)</small>
	L	H	H	H	X	NOP or BST	NOP or power down <small>(Note 8)</small>
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL <small>(Note 9)</small>
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL <small>(Note 9)</small>
	L	L	H	H	BA/RA	ACT	Row activating
	L	L	H	L	BA	PRE/PALL	NOP
	L	L	L	H	X	REF/SELF	Refresh or self refresh <small>(Note 10)</small>
	L	L	L	L	Op-Code	MRS	Mode register accessing
Row Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP or BST	NOP
	L	H	L	H	BA/CA/A10	READ/READA	Begin read: depends AP <small>(Note 11)</small>
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write: depends AP <small>(Note 11)</small>
	L	L	H	H	BA/RA	ACT	ILLEGAL <small>(Note 9)</small>
	L	L	H	L	BA	PRE/PALL	Pre-charge <small>(Note 12)</small>
	L	L	L	H	X	REF/SELF	ILLEGAL <small>(Note 10)</small>
	L	L	L	L	Op-Code	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end → Row active
	L	H	H	H	X	NOP	Continue burst to end → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, new read: AP <small>(Note 13)</small>
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, start write: AP <small>(Note 13, 14)</small>
	L	L	H	H	BA/RA	ACT	ILLEGAL <small>(Note 9)</small>
	L	L	H	L	BA	PRE/PALL	Terminate burst, pre-charging <small>(Note 10)</small>
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue the burst
	L	H	H	H	X	NOP	Continue the burst
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, start read: AP <small>(Note 13, 14)</small>
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, new write: AP <small>(Note 13)</small>
	L	L	H	H	BA/RA	ACT	ILLEGAL <small>(Note 9)</small>
	L	L	H	L	BA	PRE/PALL	Terminate burst, precharge <small>(Note 15)</small>
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

H = High level, L = Low level, X = High or Low level (Don't care)

2. Operative Command Table (Continued) (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	Continue burst to end → precharging
	L	H	H	H	X	NOP	Continue burst to end → precharging
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
Write with AP	L	L	L	L	Op-Code	MRS	ILLEGAL
	H	X	X	X	X	DESL	Continue burst to end → Write recovering with auto precharge
	L	H	H	H	X	NOP	Continue burst to end → Write recovering with auto precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
Precharging	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
	H	X	X	X	X	DESL	NOP → Enter idle after t_{RP}
	L	H	H	H	X	NOP	NOP → Enter idle after t_{RP}
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	NOP → Enter idle after t_{RP}
Row Activating	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
	H	X	X	X	X	DESL	NOP → Row active after t_{RCD}
	L	H	H	H	X	NOP	NOP → Row active after t_{RCD}
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9, 16)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Precharge

2. Operative Command Table (Continued) (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	NOP → Enter row active after t_{DPL}
	L	H	H	H	X	NOP	NOP → Enter row active after t_{DPL}
	L	H	L	H	BA/CA/A10	READ/READA	Start read, Determine AP
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP (Note 14)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write Recovering with AP	H	X	X	X	X	DESL	NOP → Enter precharge after t_{DPL}
	L	H	H	H	X	NOP	NOP → Enter precharge after t_{DPL}
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9, 14)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Refreshing	H	X	X	X	X	DESL	NOP → Enter idle after t_{RC}
	L	H	H	X	X	NOP/BST	NOP → Enter idle after t_{RC}
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL
	L	H	L	L	BA/CA/A10	READ/WRIT	ILLEGAL
	L	L	H	H	BA/RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	ACT/PRE/PALL	ILLEGAL
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	REF/SELF/MRS	ILLEGAL
Mode Register Accessing	H	X	X	X	X	DESL	NOP → Enter idle after 2 clock cycle
	L	H	H	H	X	NOP/BST	NOP → Enter idle after 2 clock cycle
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL
	L	H	L	L	BA/CA/A10	READ/WRIT	ILLEGAL
	L	L	H	H	BA/RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	ACT/PRE/PALL	ILLEGAL
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	REF/SELF/MRS	ILLEGAL

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 7: All entries assume that CKE was active (High level) during the preceding clock cycle.

Note 8: If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode.
All input buffers except CKE will be disabled.

Note 9: Illegal to bank in specified states;

Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 10: If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode.
All input buffers except CKE will be disabled.

Note 11: Illegal if t_{RCD} is not satisfied.

Note 12: Illegal if t_{RAS} is not satisfied.

Note 13: Must satisfy burst interrupt condition.

Note 14: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 15: Must mask preceding data which don't satisfy t_{DPL} .

Note 16: Illegal if t_{RRD} is not satisfied.

3. Command Truth Table for CKE

Current State	CKE		/CS	/R	/C	/W	Addr.	Action
	n-1	n						
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh with Device De-select
	L	H	L	H	H	H	X	Exit Self Refresh with No Operation
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	L	X	X	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	Maintain self refresh
Power Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit power down mode, all banks idle
	L	H	L	H	H	H	X	
	L	H	L	L	X	X	X	ILLEGAL
	L	H	L	X	L	X	X	ILLEGAL
	L	H	L	X	X	L	X	ILLEGAL
	L	L	X	X	X	X	X	Maintain power down mode
Deep Power Down	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit deep power down mode
	L	L	X	X	X	X	X	Maintain deep power down mode
All Banks Idle	H	H	H	X	X	X		Refer to operations in Operative Command Table
	H	H	L	H	X	X		
	H	H	L	L	H	X		
	H	H	L	L	L	H	X	Auto refresh
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
	H	L	H	X	X	X		
	H	L	L	H	X	X		
	H	L	L	L	H	X		
	H	L	L	L	L	H	X	Entry self refresh <i>(Note 17)</i>
	H	L	L	L	L	L	Op-Code	Mode register set
L	X	X	X	X	X	X	Power down <i>(Note 17)</i>	
Any State Other than Listed above	H	H	X	X	X	X		Refer to operations in Operative Command Table
	H	L	X	X	X	X	X	Begin clock suspend next cycle <i>(Note 18)</i>
	L	H	X	X	X	X	X	Exit clock suspend next cycle
	L	L	X	X	X	X	X	Maintain clock suspend

H = High level, L = Low level, X = High or Low level (Don't care)

Notes 17: Self refresh can be entered only from the both banks idle state.

Power down can be entered only from both banks idle or row active state.

Notes 18: Must be legal command as defined in Operative Command Table

