Revision History

Revision 0.1 (Jun. 2012)
- First release.

512Mb (8M·4Bank·16) Mobile Synchronous DRAM

Features

- Fully Synchronous to Positive Clock Edge
- VDD= 1.7 ~1.95V for 133/166MHz Power Supply
- LVCMOS Compatible with Multiplexed Address
- Programmable Burst Length (B/L) - 1, 2, 4, 8 or Full Page
- Programmable CAS Latency (C/L) - 3
- Data Mask (DQM) for Read / Write Masking
- Programmable Wrap Sequence
  – Sequential (B/L = 1/2/4/8/full Page)
  – Interleave (B/L = 1/2/4/8)
- Burst Read with Single-bit Write Operation
- All Inputs are sampled at the Rising Edge of the System Clock
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms (7.8us)
- Driver strength: normal/weak

Description

The EM48BM1684LBC is Mobile Synchronous Dynamic Random Access Memory (SDRAM) organized as 8Meg words x 4 banks by 16 bits. All inputs and outputs are synchronized with the positive edge of the clock.

The 512Mb Mobile SDRAM uses synchronized pipelined architecture to achieve high speed data transfer rates and is designed to operate at 1.8V low power memory system. It also provides auto refresh with power saving / down mode. All inputs and outputs voltage levels are compatible with LVCMOS.

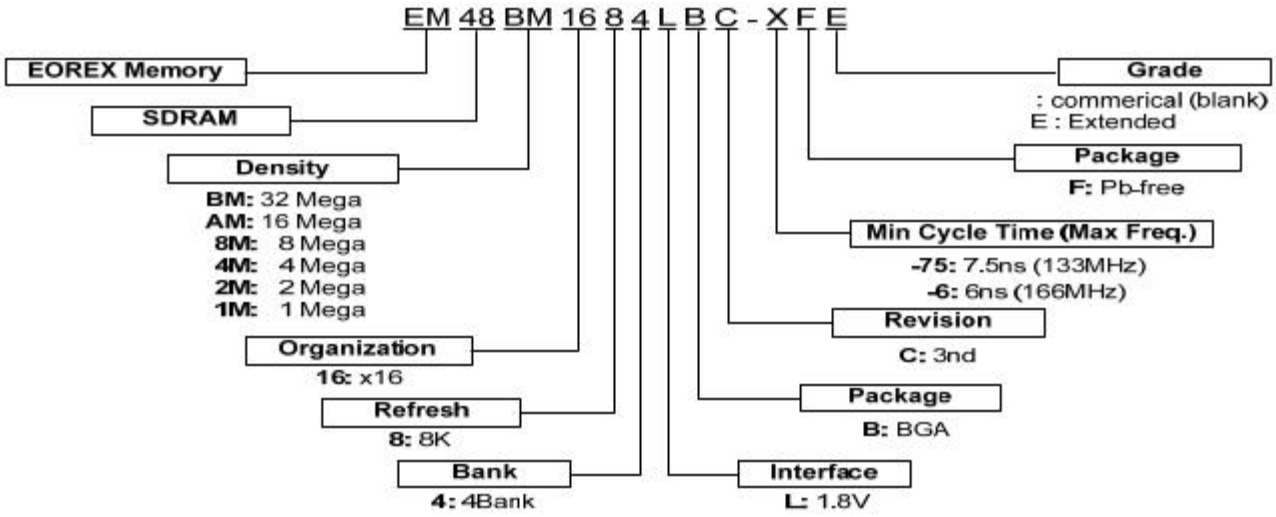
Available packages:

FBGA-54B (8mm x 9mm)

Ordering Information

Part No	Organization	Max. Freq	Package	Grade	Pb
EM48BM1684LBC-75F	32M X 16	133MHz @CL3	FBGA-54B	Commercial	Free
EM48BM1684LBC-75FE	32M X 16	133MHz @CL3	FBGA-54B	Extended	Free
EM48BM1684LBC-6F	32M X 16	166MHz @CL3	FBGA-54B	Commercial	Free
EM48BM1684LBC-6FE	32M X 16	166MHz @CL3	FBGA-54B	Extended	Free

Parts Naming Rule



* EOREX reserves the right to change products or specification without notice.

Pin Assignment: FBGA 54Ball

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	/CAS	/RAS	/WE
A12	A11	A9	G	BA0	BA1	/CS
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

54Ball FBGA (8mm x 10mm)

Pin Description (Simplified)

Pin	Name	Function
F2	CLK	**(System Clock)** Master clock input (Active on the positive rising edge)
G9	/CS	**(Chip Select)** Selects chip when active
F3	CKE	**(Clock Enable)** Activates the CLK when “H” and deactivates when “L”. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
H7,H8,J8,J7,J3, J2,H3,H2,H1,G3, H9,G2,G1	A0~A12	**(Address)** Row address (A0 to A12) is determined by A0 to A12 level at the bank active command cycle CLK rising edge. CA (CA0 to CA9) is determined by A0 to A9 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the pre-charge mode. When A10= High at the pre-charge command cycle, all banks are pre-charged. But when A10= Low at the pre-charge command cycle, only the bank that is selected by BA0/BA1 is pre-charged.
G7,G8	BA0, BA1	**(Bank Address)** Selects which bank is to be active.
F8	/RAS	**(Row Address Strobe)** Latches Row Addresses on the positive rising edge of the CLK with /RAS “L”. Enables row access & pre-charge.
F7	/CAS	**(Column Address Strobe)** Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
F9	/WE	**(Write Enable)** Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
F1, E8	UDQM, LDQM	**(Data Input/Output Mask)** DQM controls I/O buffers.
A8,B9,B8,C9,C8, D9,D8,E9,E1,D2, D1,C2,C1,B2,B1, A2	DQ0~DQ15	**(Data Input/Output)** DQ pins have the same function as I/O pins on a conventional DRAM.
A9,E7,J9/ A1,E3,J1	V_{DD}/V_{SS}	**(Power Supply/Ground)** V_{DD} and V_{SS} are power supply pins for internal circuits.
A7,B3,C7,D3/ A3,B7,C3,D7	V_{DDQ}/V_{SSQ}	**(Power Supply/Ground)** V_{DDQ} and V_{SSQ} are power supply pins for the output buffers.
E2	NC	**(No Connection)** This pin is recommended to be left No Connection on the device.

Absolute Maximum Rating

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.3 ~ +2.7		V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.3 ~ +2.7		V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +70	°C
		Extended	-25 ~ +85	
T_{STG}	Storage Temperature Range	-55 ~ +125		°C
P_D	Power Dissipation	1		W
I_{OS}	Short Circuit Current	50		mA

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (V_{CC}=1.7~1.95V, f=1MHz, T_A=25°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{CLK}	Clock Capacitance	1.5	-	3.5	pF
C_I	Input Capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML, DQMU	1.5	-	3.0	pF
C_O	Input/Output Capacitance	3.0	-	5.0	pF

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.7	1.8	1.95	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	1.7	1.8	1.95	V
V_{IH}	Input Logic High Voltage	0.8*V_{DDQ}	-	V_{DDQ}+0.3	V
V_{IL}	Input Logic Low Voltage	-0.3	-	0.3	V

Note: * All voltages referred to V_{SS}.

Recommended DC Operating Conditions

(V_{DD}=1.8V)

Symbol	Parameter	Test Conditions	Speed -6	Speed -75	Units
I_{DD1}	Operating Current ***(Note 1)***	Burst length=1, t_{RC}=t_{RC}(min.), I_{OL}=0mA, One bank active	38	35	mA
I_{DD2P}	Precharge Standby Current in Power Down Mode	CKE≦V_{IL}(max), t_{CK}=15ns	0.8	0.8	mA
I_{DD3P}	Active Standby Current in Power Down Mode	CKE≦V_{IL}(max), t_{CK}=15ns	5	5	mA
I_{CC4}	Operating Current (Burst Mode) ***(Note 2)***	t_{CCD}≧2t_{CK}, I_{OL}=0mA	75	70	mA
I_{CC5}	Auto Refresh Current ***(Note 3)***	CKE, /CS=high, t_{RFC}≧t_{RFC} (MIN)	75	75	mA
I_{CC6}	Self Refresh Current	CKE≦0.2V, Full Array	1	1	mA

*All voltages referenced to V_{SS}.

Note 1: I_{CC1} depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during t_{CK} (min.)

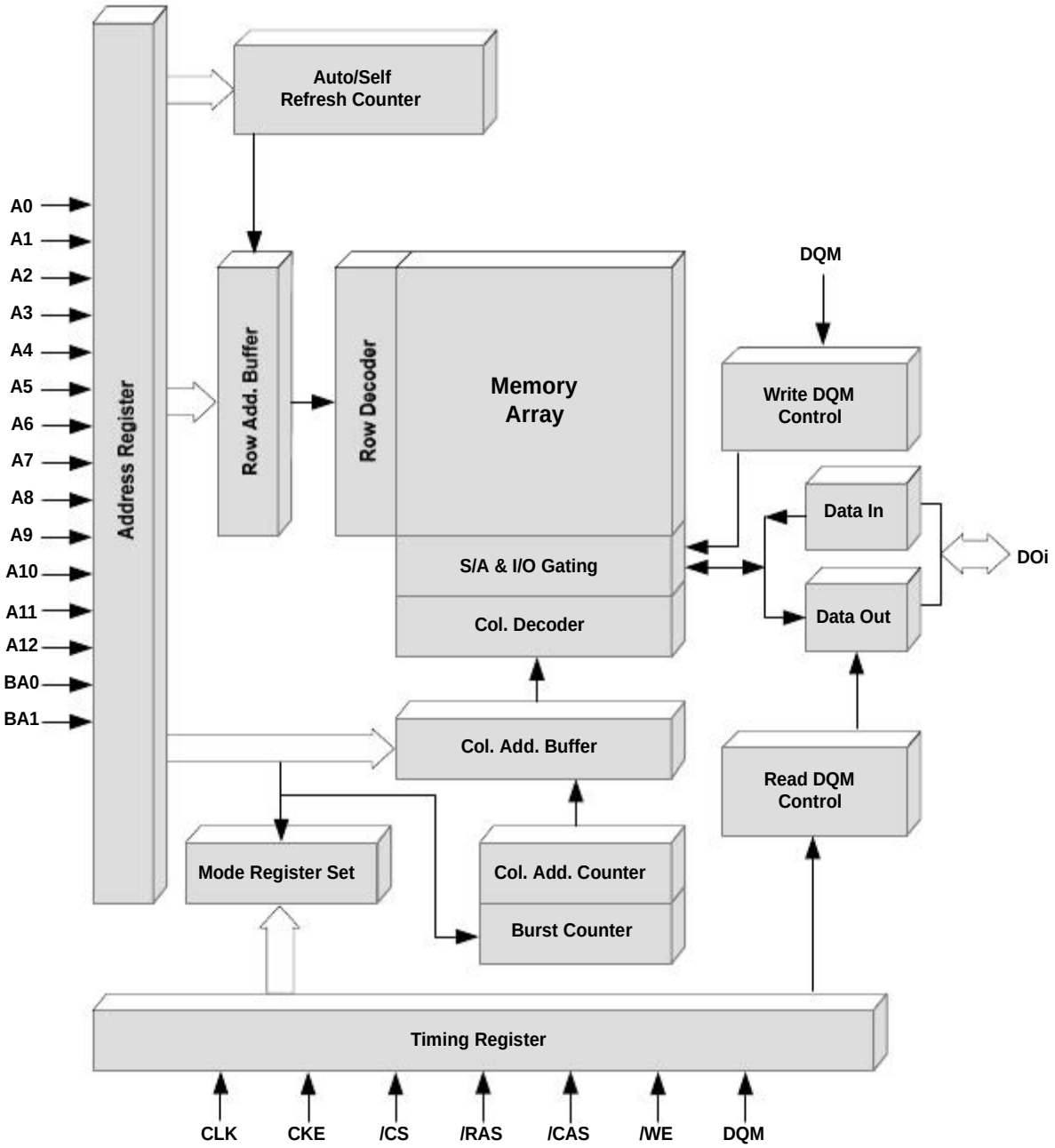
Note 2: I_{CC4} depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during t_{CK} (min.)

Note 3: Input signals are changed only one time during t_{CK} (min.)

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{IL}	Input Leakage Current	0≦V_I≦V_{DDQ}, V_{DDQ}=V_{DD} All other pins not under test=0V	-1	-	+1	uA
I_{OL}	Output Leakage Current	0≦V_O≦V_{DDQ}, D_{OUT} is disabled	-5	-	+5	uA
V_{OH}	High Level Output Voltage	I_O=-0.1mA	0.9*V_{DDQ}	-	-	V
V_{OL}	Low Level Output Voltage	I_O=+0.1mA	-	-	0.2	V

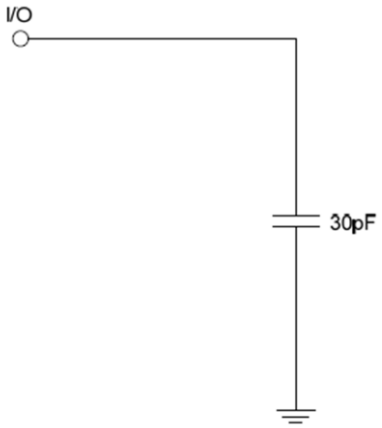
Block Diagram



AC Operating Test Conditions

(V_{DD}=1.8V)

Item	Conditions
Output Reference Level	0.5*VDDQ
Output Load	See diagram as below
Input Signal Level	0.9*VDDQ/0.2
Transition Time of Input Signals	1ns/1ns
Input Reference Level	0.5*VDDQ



AC Operating Test Characteristics

(V_{DD}=1.8V)

Symbol	Parameter		-6		-75		Units
			Min	Max	Min	Max	
t_{CK}	Clock Cycle Time	CL=3	6	-	7.5	-	ns
t_{AC}	Access Time form CLK	CL=3	-	5.4	-	5.4	ns
t_{CH}	CLK High Level Width		2	-	2.5	-	ns
t_{CL}	CLK Low Level Width		2	-	2.5	-	ns
t_{OH}	Data-out Hold Time	CL=3	2.5	-	2.5	-	ns
t_{HZ}	Data-out High Impedance Time ***(Note 5)***	CL=3	-	5.4	-	5.4	ns
t_{LZ}	Data-out Low Impedance Time		1	-	1	-	ns
t_{IH}	Input Hold Time		1	-	1	-	ns
t_{IS}	Input Setup Time		1.5	-	1.5	-	ns

* All voltages referenced to V_{SS}.

Note 5: t_{HZ} defines the time at which the output achieve the open circuit condition and is not referenced to output voltage levels.

AC Operating Test Characteristics (Continued)

(V_{DD}=1.8V)

Symbol	Parameter		-6		-75		Units
			Min.	Max.	Min.	Max.	
t_{RC}	ACTIVE to ACTIVE Command Period ***(Note 6)***		60	-	72.5	-	ns
t_{RAS}	ACTIVE to PRECHARGE Command Period ***(Note 6)***		42	100k	50	100k	ns
t_{RP}	PRECHARGE to ACTIVE Command Period ***(Note 6)***		18	-	18	-	ns
t_{RCD}	ACTIVE to READ/WRITE Delay Time ***(Note 6)***		18	-	18	-	ns
t_{RRD}	ACTIVE(one) to ACTIVE(another) Command ***(Note 6)***		12	-	15	-	ns
t_{CCD}	READ/WRITE Command to READ/WRITE Command		1	-	1	-	t_{CLK}
t_{DPL}	Date-in to PRECHARGE Command		2	-	2	-	t_{CLK}
t_{BDL}	Date-in to BURST Stop Command		1	-	1	-	t_{CLK}
t_{ROH}	Data-out to High Impedance from PRECHARGE Command	CL=3	3	-	3	-	t_{CLK}
t_{REF}	Refresh Time (8,192 cycle)		-	64	-	64	ms
t_{RFC}	Refresh to Refresh/ACTIVE command period		72	-	72	-	ns

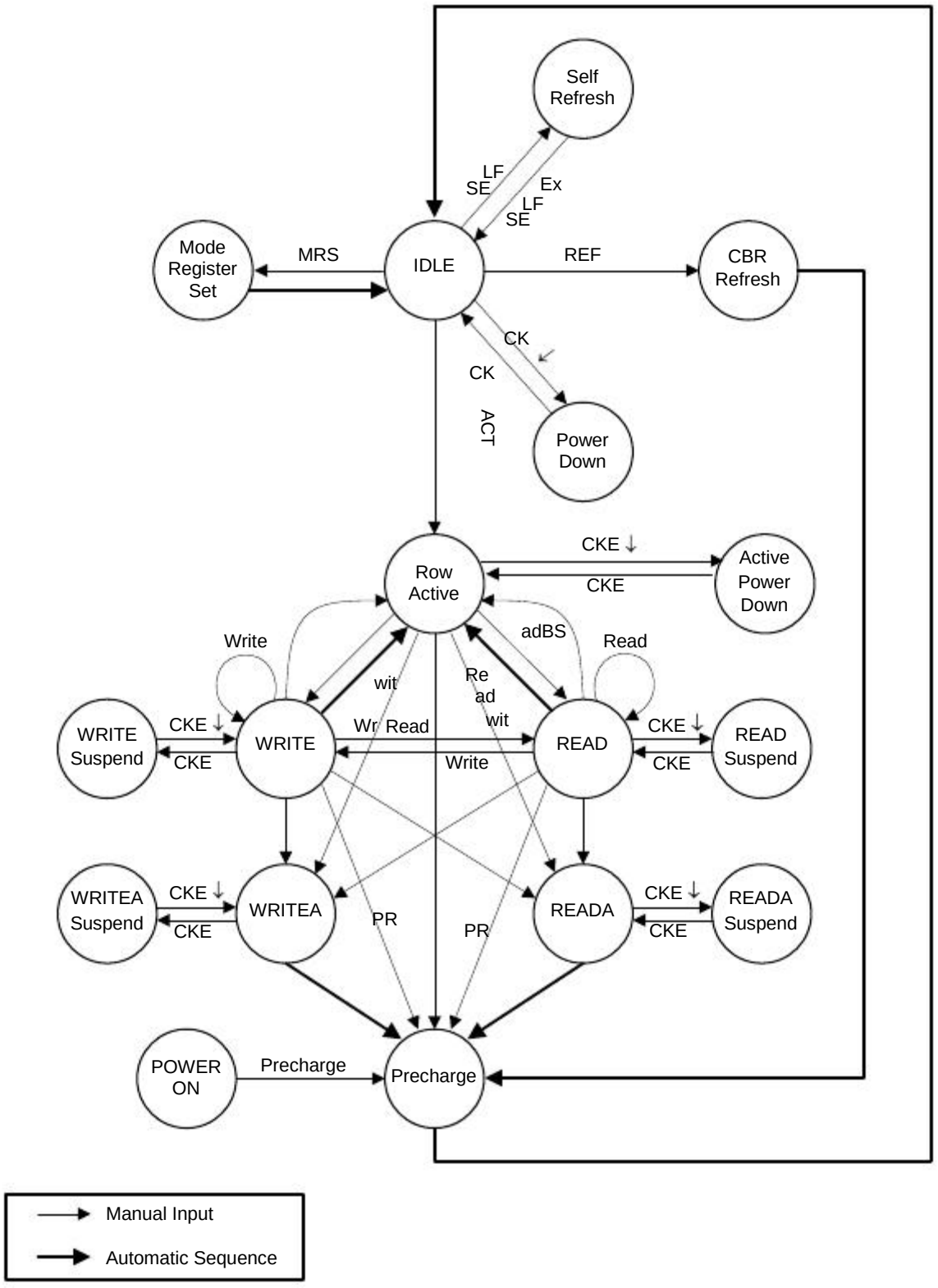
* All voltages referenced to V_{SS}.

Note 6: These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows:
The number of clock cycles = Specified value of timing/clock period (Count Fractions as a whole number)

Recommended Power On and Initialization

The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs. (Like a conventional DRAM) During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed V_{DD}+0.3V on any of the input pins or V_{DD} supplies. (CLK signal started at same time)
After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command.
To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required, and these may be done before or after programming the Mode Register.

Simplified State Diagram



Address Input for Mode Register Set

BA1	BA0	A12/A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Operation Mode							CAS Latency			BT	Burst Length		

Burst Length				
Sequential	Interleave	A2	A1	A0
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
Reserved	Reserved	1	0	0
Reserved	Reserved	1	0	1
Reserved	Reserved	1	1	0
Full Page	Reserved	1	1	1

Burst Type	A3
Interleave	1
Sequential	0

CAS Latency	A6	A5	A4
Reserved	0	0	0
Reserved	0	0	1
Reserved	0	1	0
3	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

BA1	BA0	A12/A11	A10	A9	A8	A7	Operation Mode
0	0	0	0	0	0	0	Normal
0	0	0	0	1	0	0	Burst Read with Single-bit Write

Burst Type (A3)

Burst Length	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	0	01	01
	X	X	0	10	10
4	X	0	0	0123	0123
	X	0	1	1230	1032
	X	1	0	2301	2301
	X	1	1	3012	3210
8	0	0	0	01234567	01234567
	0	0	1	12345670	10325476
	0	1	0	23456701	23016745
	0	1	1	34567012	32107654
	1	0	0	45670123	45670123
	1	0	1	56701234	54761032
	1	1	0	67012345	67452301
	1	1	1	70123456	76543210
Full Page*	n	n	n	Cn Cn+1 Cn+2……	-

* Page length is a function of I/O organization and column addressing -16 (CA0 ~ CA8):

Full page = 1024bits

1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A11, A9~A10
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	X	L	H	L	L	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. DQM Truth Table

Command	Symbol	CKE		/CS
		n-1	n	
Data Write/Output Enable	ENB	H	X	H
Data Mask/Output Disable	MASK	H	X	L
Upper Byte Write Enable/Output Enable	BSTH	H	X	L
Read	READ	H	X	L
Read with Auto Pre-charge	READA	H	X	L
Write	WRIT	H	X	L
Write with Auto Pre-charge	WRITA	H	X	L
Bank Activate	ACT	H	X	L
Pre-charge Select Bank	PRE	H	X	L
Pre-charge All Banks	PALL	H	X	L
Mode Register Set	MRS	H	X	L

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

3. CKE Truth Table

Item	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Activating	Clock Suspend Mode Entry		H	L	X	X	X	X	X
Any	Clock Suspend Mode		L	L	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit		L	H	X	X	X	X	X
Idle	CBR Refresh Command	REF	H	H	L	L	L	H	X
Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power Down Entry		H	L	X	X	X	X	X
Power Down	Power Down Exit		L	H	X	X	X	X	X

Remark H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	Nop or power down (Note 8)
	L	H	H	X	X	NOP or BST	Nop or power down (Note 8)
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	Row activating
	L	L	H	L	BA, A10	PRE/PALL	Nop
	L	L	L	H	X	REF/SELF	Refresh or self refresh (Note 10)
	L	L	L	L	Op-Code	MRS	Mode register accessing
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	X	X	NOP or BST	Nop
	L	H	L	H	BA/CA/A10	READ/READA	Begin read: Determine AP (Note 11)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write: Determine AP (Note 11)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Pre-charge (Note 12)
	L	L	L	H	X	REF/SELF	ILLEGAL (Note 10)
	L	L	L	L	Op-Code	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end → Row active
	L	H	H	H	X	NOP	Continue burst to end → Row active
	L	H	H	L	X	BST	Burst stop → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, new read: Determine AP (Note 13)
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, start write: Determine AP (Note 13, 14)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, pre-charging (Note 10)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end → Write recovering
	L	H	H	H	X	NOP	Continue burst to end → Write recovering
	L	H	H	L	X	BST	Burst stop → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, start read: Determine AP 7, 8 (Note 13, 14)
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, new write: Determine AP 7 (Note 13)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, pre-charging (Note 15)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table (Continued) (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	Continue burst to end → Pre-charging
	L	H	H	H	X	NOP	Continue burst to end → Pre-charging
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write with AP	H	X	X	X	X	DESL	Burst to end → Write recovering with auto pre-charge
	L	H	H	H	X	NOP	Continue burst to end → Write recovering with auto pre-charge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Pre-charging	H	X	X	X	X	DESL	Nop → Enter idle after t_{RP}
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RP}
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Row Activating	H	X	X	X	X	DESL	Nop → Enter idle after t_{RCD}
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RCD}
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9, 16)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

4. Operative Command Table (Continued) (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	Nop → Enter row active after t_{DPL}
	L	H	H	H	X	NOP	Nop → Enter row active after t_{DPL}
	L	H	H	L	X	BST	Nop → Enter row active after t_{DPL}
	L	H	L	H	BA/CA/A10	READ/READA	Start read, Determine AP
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP *(Note 14)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 9)*
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL *(Note 9)*
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write Recovering with AP	H	X	X	X	X	DESL	Nop → Enter pre-charge after t_{DPL}
	L	H	H	H	X	NOP	Nop → Enter pre-charge after t_{DPL}
	L	H	H	L	X	BST	Nop → Enter pre-charge after t_{DPL}
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL *(Note 9, 14)*
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL *(Note 9)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 9)*
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Refreshing	H	X	X	X	X	DESL	Nop → Enter idle after t_{RC}
	L	H	H	X	X	NOP/BST	Nop → Enter idle after t_{RC}
	L	H	L	X	X	READ/WRIT	ILLEGAL
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL
Mode Register Accessing	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	X	X	READ/WRIT	ILLEGAL
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 7: All entries assume that CKE was active (High level) during the preceding clock cycle.

Note 8: If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode. All input buffers except CKE will be disabled.

Note 9: Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 10: If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode. All input buffers except CKE will be disabled.

Note 11: Illegal if t_{RCD} is not satisfied.

Note 12: Illegal if t_{RAS} is not satisfied.

Note 13: Must satisfy burst interrupt condition.

Note 14: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 15: Must mask preceding data which don't satisfy t_{DPL}.

Note 16: Illegal if t_{RRD} is not satisfied.

5. Command Truth Table for CKE

Current State	CKE		/CS	/R	/C	/W	Addr.	Action
	n-1	n						
Self Refresh	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit self refresh
	L	H	H	X	X	X	X	Self refresh recovery
	L	H	L	H	H	X	X	Self refresh recovery
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	Maintain self refresh
Self Refresh Recovery	H	H	H	X	X	X	X	Idle after t_{RC}
	H	H	L	H	H	X	X	Idle after t_{RC}
	H	H	L	H	L	X	X	ILLEGAL
	H	H	L	L	X	X	X	ILLEGAL
	H	L	H	X	X	X	X	ILLEGAL
	H	L	L	H	H	X	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
Power Down	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit power down
	L	H	X	X	X	X	X	Exit power down → Idle
	L	L	X	X	X	X	X	Maintain power down mode
Both Banks Idle	H	H	H	X	X	X		Refer to operations in Operative Command Table
	H	H	L	H	X	X		
	H	H	L	L	H	X		
	H	H	L	L	L	H	X	Refresh
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
	H	L	H	X	X	X		
	H	L	L	H	X	X		
	H	L	L	L	H	X		
	H	L	L	L	L	H	X	Self refresh ***(Note 17)***
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
	L	X	X	X	X	X	X	Power down ***(Note 17)***
Row Active	H	X	X	X	X	X	X	Refer to operations in Operative Command Table
	L	X	X	X	X	X	X	Power down ***(Note 17)***
Any State Other than Listed above	H	H	X	X	X	X		Refer to operations in Operative Command Table
	H	L	X	X	X	X	X	Begin clock suspend next cycle ***(Note 18)***
	L	H	X	X	X	X	X	Exit clock suspend next cycle
	L	L	X	X	X	X	X	Maintain clock suspend

Remark: H = High level, L = Low level, X = High or Low level (Don't care)

Notes 17: Self refresh can be entered only from the both banks idle state.
Power down can be entered only from both banks idle or row active state.

Notes 18: Must be legal command as defined in Operative Command Table

Package Description

Package: FBGA-54B

Unit: mm